High Power Density 650V Half-Bridge GaN Transistors with Gate Driver

General description

The CGC02002 is an advanced system-in-package (SIP) power ICs, consisting of gate driver and two 650-V enhancement-mode GaN power transistors in half-bridge configuration.

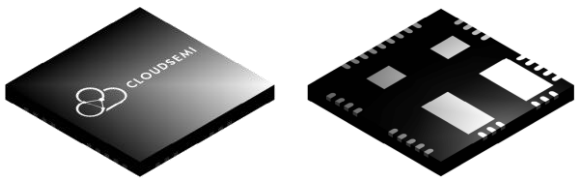
The integrated GaN power transistors have $R_{DS(on)}$ of 190 mΩ and 190 mΩ for high- and low-side and drain-source blocking voltage of 650 V.

The CGC02002 features wide power supply range. And the high-side driver can be easily supplied by bootstrap circuit. Both the high-side and low-side gate drive voltage (VDDH and VDDL) is provided by internal voltage regulator, making an easy circuit design.

The CGC02002 features UVLO function for both high-side and low-side driving sections, preventing GaN transistors from operating in low-efficiency or unsafe conditions. The programmable deadtime function can avoid cross-conduction conditions.

The input signal pin arrangement allows easy interfacing with controllers.

The CGC02002 operates in the industrial temperature range of -40 °C to 125 °C. The device is in available in 9mm*9mm QFN package.



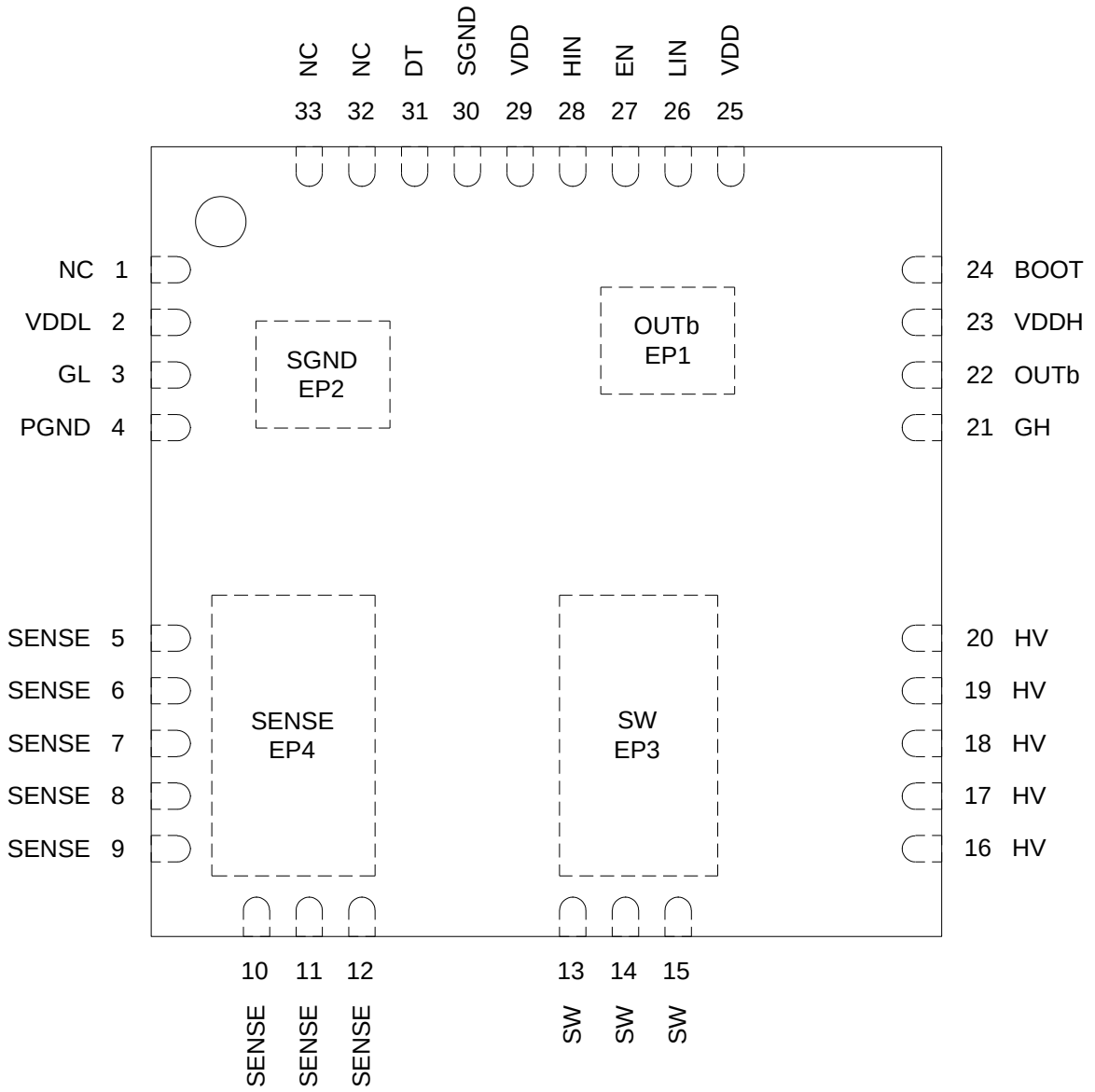
Features

- Integrated half-bridge GaN transistors with gate driver
- 650V drain-source blocking capabilities
- High/low-side $R_{DS(on)}$ of 140/190 mΩ
- Zero reverse recovery loss
- Ultra-low standby current
- Wide power supply range (10V~18V)
- Programmable deadtime (20ns~100ns)
- UVLO protections for high-side and low-side
- Over-temperature protection (OTP)
- QFN 9*9 package
- Operating temperature of -40 °C to 125 °C
- Bill of material (BOM) reduction
- Very compact and simplified layout
- Flexible and easy design

Typical applications

- Switch-mode power supplies
- Chargers and adaptors
- DC/DC, DC/AC converters
- ACF, AHB, LLC, totem-pole PFC

Pin configuration and functions



Pin list

Pin #	Name	I/O	Description
2	VDDL	P	Gate driver low-side supply voltage. A ceramic capacitor of not less than 100nF must be connected between VDDL and PGND
3	GL	O	Low-side GaN gate
4	PGND	G	Gate driver low-side drive reference, internally connected to SENSE
5,6,7,8,9,10,11,12, EP4	SENSE	P	Half-bridge sense (low-side GaN source)
13,14,15, EP3	SW	O	Half-bridge output

16,17,18,19,20	HV	P	High-voltage power supply (High side GaN drain)
21	GH	O	High-side GaN gate
22, EP1	OUTb	G	Gate driver high-side reference voltage, used only for bootstrap capacitor connection, internally connected to SW
23	VDDH	P	Gate driver high-side supply voltage. A ceramic capacitor of not less than 100nF must be connected between VDDH and OUTb
24	BOOT	P	Power supply for high-side regulator (bootstrap voltage)
25,29	VDD	P	Power supply for logic and low-side regulator
26	LIN	I	Low-side driver logic input
27	EN	I	Dual drivers enabling logic input
28	HIN	I	High-side driver logic input
30, EP2	SGND	G	Logic ground
31	DT	I	Dead-time adjustment
1,32,33	NC	NC	Leave floating

I = Input, O = Output, P = Power, G = Ground, NC = No Connect

Ordering information

Ordering No.	Description
CGC02002	QFN9*9, 2000 pcs/reel

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1 Absolute maximum ratings

At T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate product lifetime. For further information, contact CloudSemi sales office.

Parameters	Symbols	Min.	Max.	Units	Notes/Test Conditions
High-side common mode voltage	V_{SW}	-650	650	V	
Driver Supply Voltage	VDD to SGND	-0.3	24	V	
Regulator Output Voltage	VDDL to PGND, VDDH to OUTb	-0.3	7	V	
Different Ground Voltage	SGND to PGND	-5	5	V	
Input Signal Voltage	HIN, LIN, EN, DT to SGND	-0.3	V_{VDD}+0.3	V	
Input Signal Voltage, transient for 50ns	HIN, LIN, EN, DT to SGND	-5	V_{VDD}+0.3	V	
Driver Output Voltage	GL to PGND GH to OUTb	-0.3 -0.3	V_{VDDL}+0.3 V_{VDDH}+0.3	V	
Driver Output Voltage, transient for 50ns	GL to PGND GH to OUTb	-2 -2	7 7	V	
GaN drain-source voltage	$V_{DS, max}$	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
Continuous current, drain-source	I_D	-	10	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	20	A	T_c = 25 °C; V_{GS} = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	10	A	T_c = 125 °C; V_{GS} = 6 V
Operating temperature	T_j	-40	+150	°C	
Storage temperature	T_{stg}	-55	+150	°C	
Electrostatic Discharge	HBM (all pins)	-3000	3000	V	
	CDM	-1000	1000	V	

Notes

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Pulse width = 10 μs.

2 Recommended operating conditions

At T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate product lifetime. For further information, contact CloudSemi sales office.

Parameters	Symbols	Min.	Max.	Units	Notes/Test Conditions
High-side Common Mode Voltage	V_{SW}	0	600	V	
Driver Supply Voltage	VDD to SGND	10	18	V	
Driver Output Voltage	GL to PGND GH to OUTb	0 0	V_{VDDL} V_{VDDH}	V	
Input Signal Voltage	HIN, LIN, EN, DT to SGND	0	V_{VDD}	V	
High voltage bus	HV to SENSE	0	520	V	
Operating temperature	T_j	-40	+130	°C	
Ambient Temperature	Ta	-40	+125	°C	

3 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction to each GaN transistor exposed pad, typical	$R_{th(J-CB)}$	-	-	2	°C/W	
Thermal resistance junction-to-ambient	$R_{th(J-A)}$	-	-	18	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

4.1 Driver

At VDD=12V, T_j = 25 °C, unless specified otherwise.

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Driver Power Supply						
V_{DD} quiescent current	I_{VDDQ}	-	0.42	-	mA	HIN = LIN = 0 V
V_{DD} operating current	I_{VDDO}	-	1	-	mA	HV = SW = 0V, BOOT = 12V, f = 500kHz
BOOT quiescent current	I_{BOOTQ}	-	0.55	-	mA	
BOOT operating current	I_{BOOTO}	-	1.2	-	mA	HV = SW = 0V, BOOT = 12V, f = 500kHz
BOOT UVLO state quiescent current	I_{BOOTQ_OFF}	-	0.3	-	mA	BOOT-SW = 7V
VDD UVLO rising threshold	V_{VDD_ON}	8.1	8.4	8.8	V	
VDD UVLO falling threshold	V_{VDD_OFF}	7.5	7.8	8.1	V	
VDD UVLO hysteresis	V_{VDD_HYS}	0.4	0.6	-	V	
BOOT UVLO rising threshold	V_{BOOT_ON}	8.1	8.4	8.8	V	
BOOT UVLO falling threshold	V_{BOOT_OFF}	7.5	7.8	8.1	V	
BOOT UVLO hysteresis	V_{BOOT_HYS}	0.4	0.6	-	V	
Input Logic						
Input pin pull-down resistance	R_{HIN_PD}, R_{LIN_PD}	-	200	-	kΩ	HIN = LIN = 3V
Enable pin pull-down resistance	R_{EN_PD}	-	200	-	kΩ	EN = 3V
Input pin high logic bias current	I_{HIN_H}, I_{LIN_H}	-	20	-	μA	HIN = LIN = 5V
Enable pin high logic bias current	I_{EN_H}	-	20	-	μA	EN = 5V
Logic high input threshold	V_{HIN_H}, V_{LIN_H}, V_{EN_H}	1.7	2.1	2.5	V	
Logic low input threshold	V_{HIN_L}, V_{LIN_L}, V_{EN_L}	0.9	1.2	1.5	V	
Logic input hysteresis	V_{HIN_HYS}, V_{LIN_HYS}, V_{EN_HYS}	0.7	0.9	-	V	
Driver Output Characteristic						
Regulator Output Voltage	V_{VDDL}, V_{VDDH}-V_{SW}	5.7	6	6.3	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF
Regulator UVLO rising threshold	V_{VDDH_ON}, V_{VDDL_ON}	4.3	4.5	4.7	V	
Regulator UVLO falling threshold	V_{VDDH_OFF}, V_{VDDL_OFF}	3.8	4	4.2	V	
Regulator UVLO hysteresis	V_{VDDH_HYS}, V_{VDDL_HYS}	0.4	0.5	-	V	

Driver output pull-down resistance	R_{LSNK}, R_{HSNK}	-	1	-	Ω	
Driver output pull-up resistance	R_{LSRC}, R_{HSRC}	-	51	-	Ω	
Output peak source current	I_{LSRC_PK}, I_{HSRC_PK}	-	2 2	-	A	
Output peak sink current	I_{LSNK_PK}, I_{HSNK_PK}	-	4 4	-	A	

4.2 GaN power transistor

At T_j = 25 °C, unless specified otherwise.

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Low-side / High-side GaN power FET static characteristics						
Drain-source voltage	$V_{DS,\ max}$	-	-	650	V	V_{GS} = 0 V; I_D = 10 µA
Drain-source leakage current	I_{DSS}	-		20	µA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	6	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 6.6 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.7	-		I_D = 6.6 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	140	190	mΩ	V_{GS} = 6 V; I_D = 6 A; T_j = 25 °C
		-	250	-		V_{GS} = 6 V; I_D = 6 A; T_j = 150 °C
Low-side / High-side GaN power FET dynamic characteristics						
Total Gate charge	Q_G	-	2.8	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 6 A
Output charge	Q_{OSS}	-	25	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output Capacitance Stored Energy	E_{oss}	-	3.6	-	µJ	
Output capacitance	C_{oss}	-	30	-	pF	
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	41	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	63	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Notes

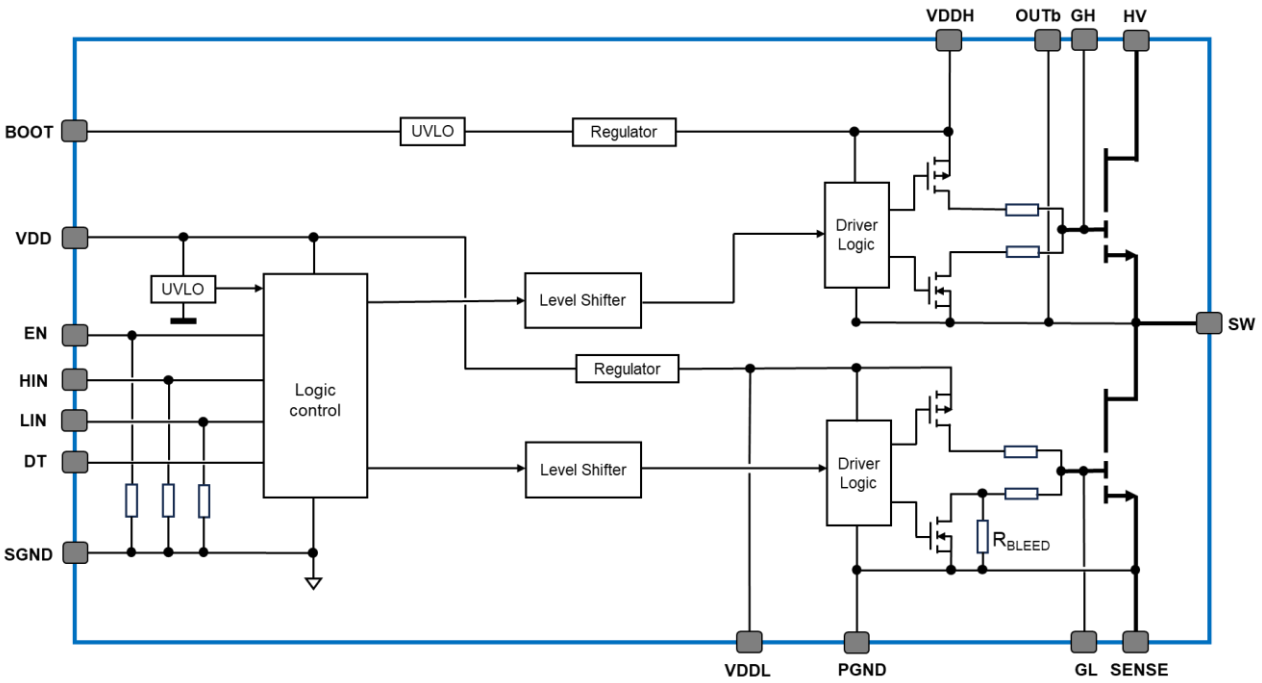
1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

4.3 Switching characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Low-side / High-side GaN power FET						
Turn-on delay time	$t_{d(on)}$	-	70	-	ns	HV = 400V V_{GS} = 6 V I_D = 6 A
Turn-on rise time	$t_{r(on)}$	-	15	-	ns	
Turn-off delay time	$t_{d(off)}$	-	70	-	ns	
Turn-off fall time	$t_{f(off)}$	-	15	-	ns	

5 Block diagram



6 Switching waveforms

Figure 6.1 shows the circuit used to measure the GaN power FET switching parameters. The circuit is operated as a double-pulse tester. Consult external references for double-pulse tester details. The circuit is placed in the boost configuration to measure the low-side GaN switching parameters. The circuit is placed in the buck configuration to measure the high-side GaN switching parameters. The GaN FET not being measured in each configuration (high-side in the boost and low-side in the buck) acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode. Table 6.1 shows the details for each configuration.

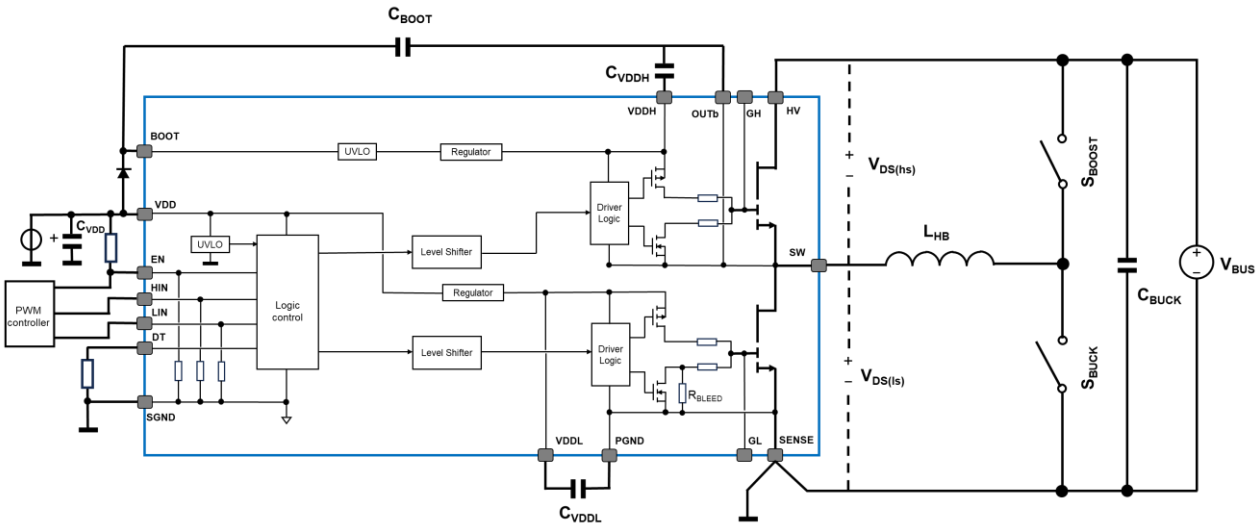


Figure 6.1 GaN power FET switching parameters test circuit

Table 6.1 GaN power FET switching parameters test circuit configuration details

Configuration	GaN FET under test	GaN FET Acting as diode	S_{BOOST}	S_{BUCK}	V_{LIN}	V_{HIN}
Boost	Low-side	High-side	Closed	Open	Double-pulse waveform	0V
Buck	High-side	Low-side	Open	Closed	0V	Double-pulse waveform

Figure 6.2 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. Note that the turn-on rise time is the same as the VDS 80% to 20% fall time.

The GaN power FET turn-off transition has two timing components: turn-off delay time, and turn-off fall time. Note that the turn-off fall time is the same as the VDS 20% to 80% rise time.

The turn-on slew rate is measured over a smaller voltage delta (100 V) compared to the turn-on rise time voltage delta (240 V) to obtain a faster slew rate which is useful for EMI design.

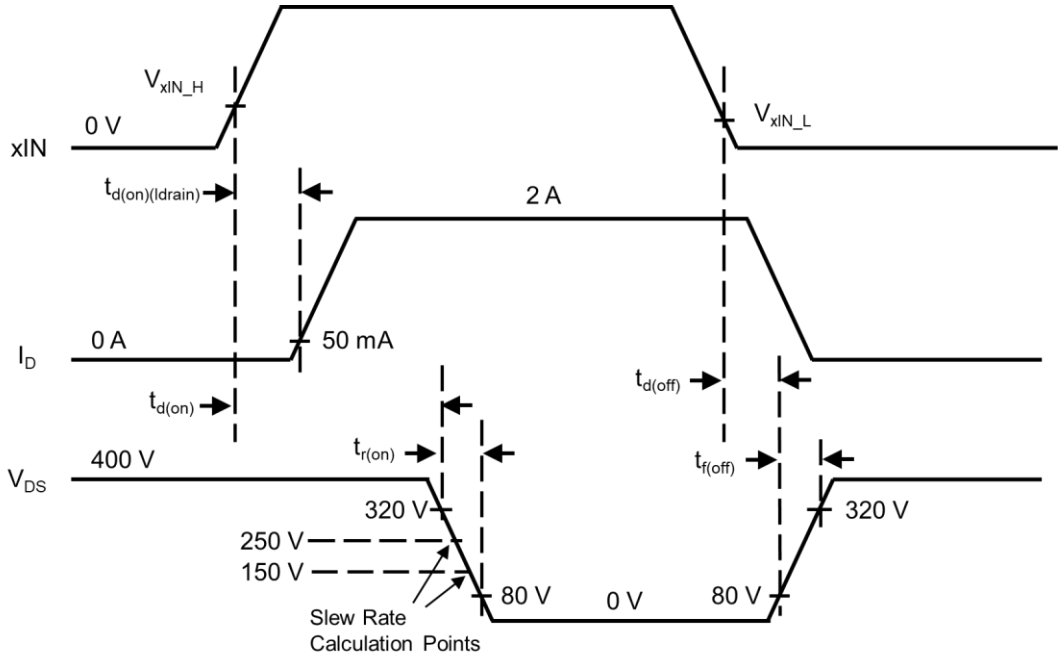
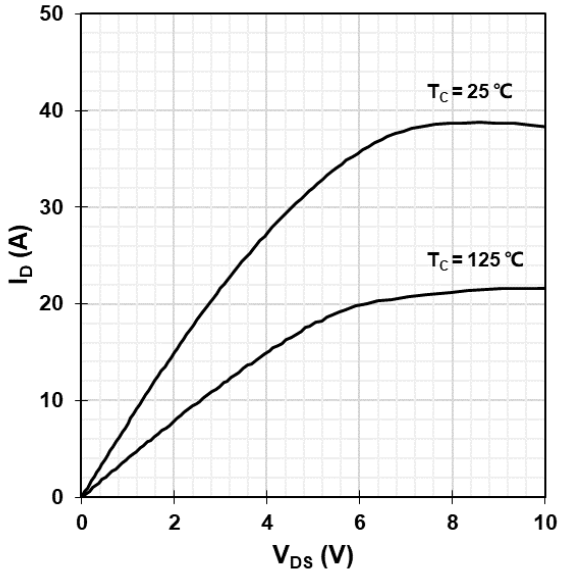


Figure 6.2 GaN power FET switching parameters

7 Electrical characteristics diagrams

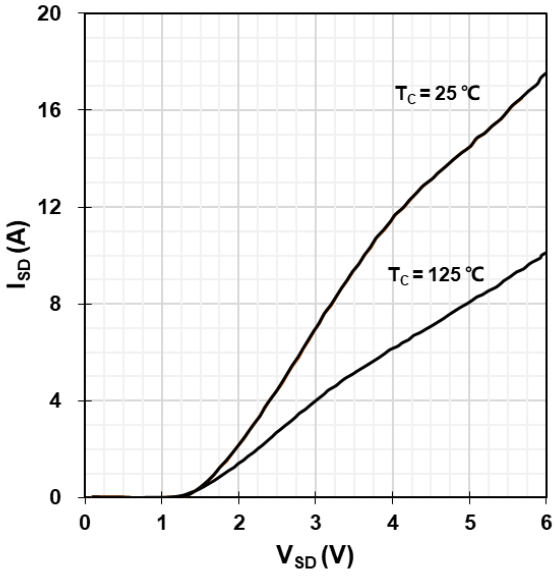
At T_j = 25 ºC, unless specified otherwise.

Figure 1 Typ. output characteristics



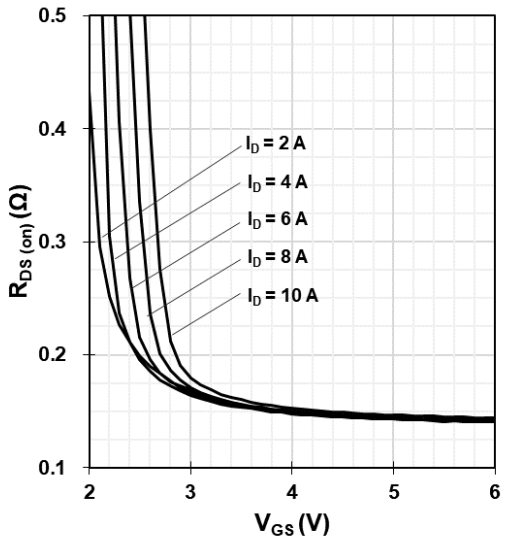
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 ºC

Figure 2 Typ. output characteristics



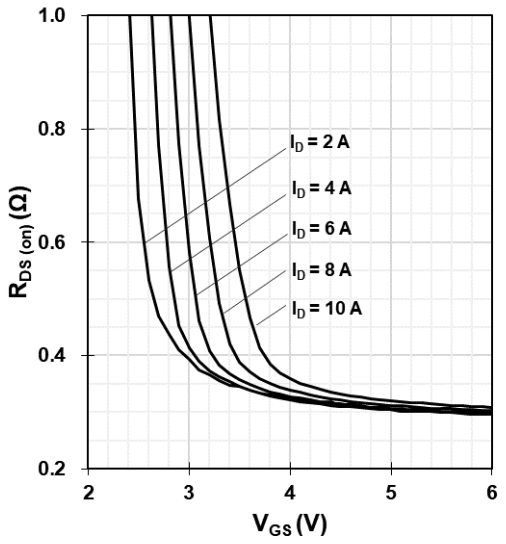
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 ºC

Figure 3 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 25 ºC

Figure 4 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 125 ºC

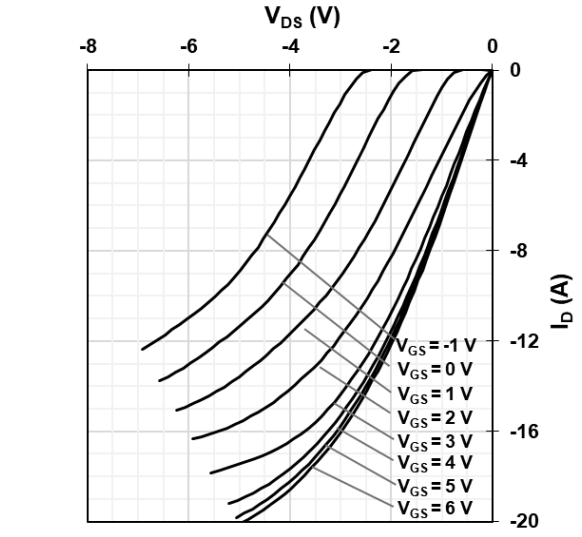
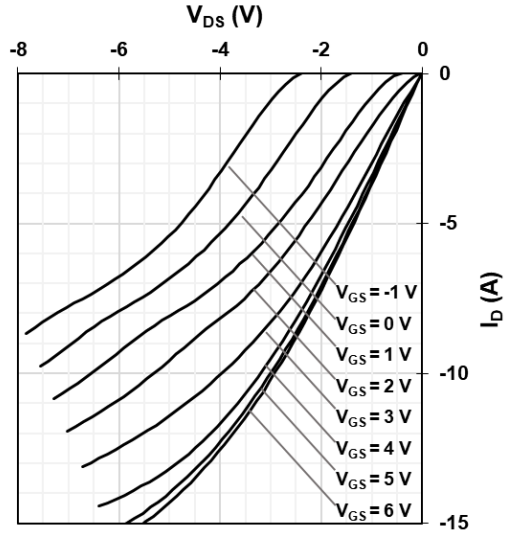
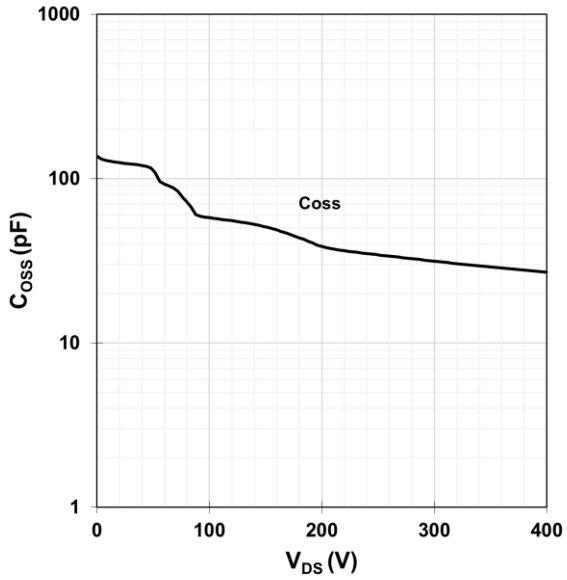
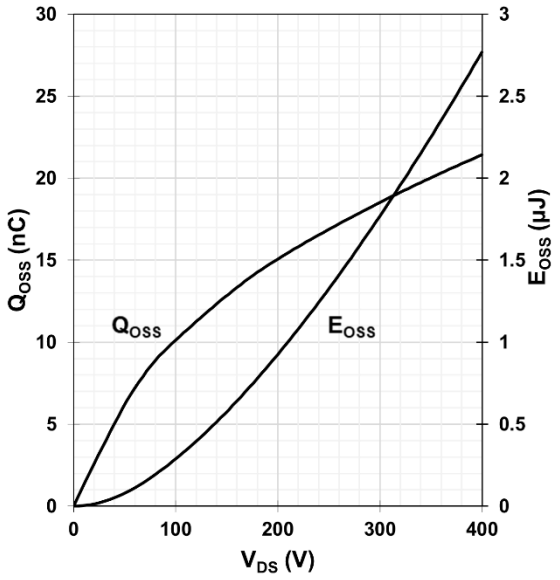
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. output capacitance	Figure 8 Typ. C_{oss} stored charge & energy
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

8 Function description

8.1 Under Voltage Lock Out (UVLO)

The CGC02002 has internal under voltage lock out (UVLO) protections on low side and high side power supply blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDD or BOOT is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The 0.5V hysteresis (V_{VDD_HYS}) on VDD and BOOT ULVO protections are provided prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup. The recovery propagation time of V_{VDDL} is about 1us when V_{VDD} voltage fall from more than V_{VDD_ON} to some value between V_{VDD_OFF} and V_{VDD_POR} and then raise to more than V_{VDD_ON}.

A not less than 100nF ceramic capacitor must be used on VDDL and VDDH to normally operate.

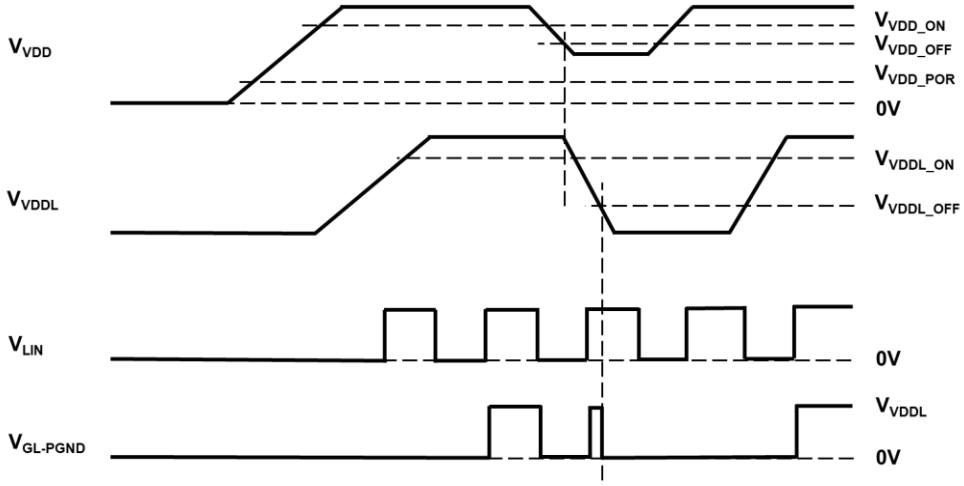


Figure 8.1 UVLO Diagram

8.2 Input and Output Logic

The CGC02002 an advanced system-in-package (SIP) power ICs, consisting of gate driver and two 650-V enhancement-mode GaN power transistors in half-bridge configuration with dead-time control. The EN pin should be logic high to keep the driver operating normally.

Table 8.1 Inputs truth table (applicable when device is not in UVLO)

Input Pins			Output Pins		Note
EN	**LIN**	**HIN**	**LS**	**HS**	
L or O	X	X	OFF	OFF	
H	L	L	OFF	OFF	
H	L	H	OFF	**ON**	
H	H	L	**ON**	OFF	
H	H	H	OFF	OFF	The input signal is later than VDD power up.

Notes: H = Logic High; L = Logic Low; O = Left Open; X = Irrelevant.

8.3 Programmable Deadtime (DT pin)

The CGC02002 has a programmable deadtime control function by placing a resistor, R_{DT}, between the DT pin and SGND. There are three statuses of deadtime program.

1) While R_{DT} is lower than 20kΩ or higher than 250kΩ, the deadtime duration (t_{DT}) is set to 20ns.

2) While R_{DT} is in range of 20kΩ to 100kΩ, the t_{DT} can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 1 \times R_{DT} \quad (1)$$

3) While R_{DT} is in range of 100 kΩ to 250kΩ, the deadtime duration (t_{DT}) is set to 100ns.

The recommended value of R_{DT} is between from 1kΩ to 200kΩ. It is also recommended to parallel a ceramic capacitor, for example 1nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 8.2:

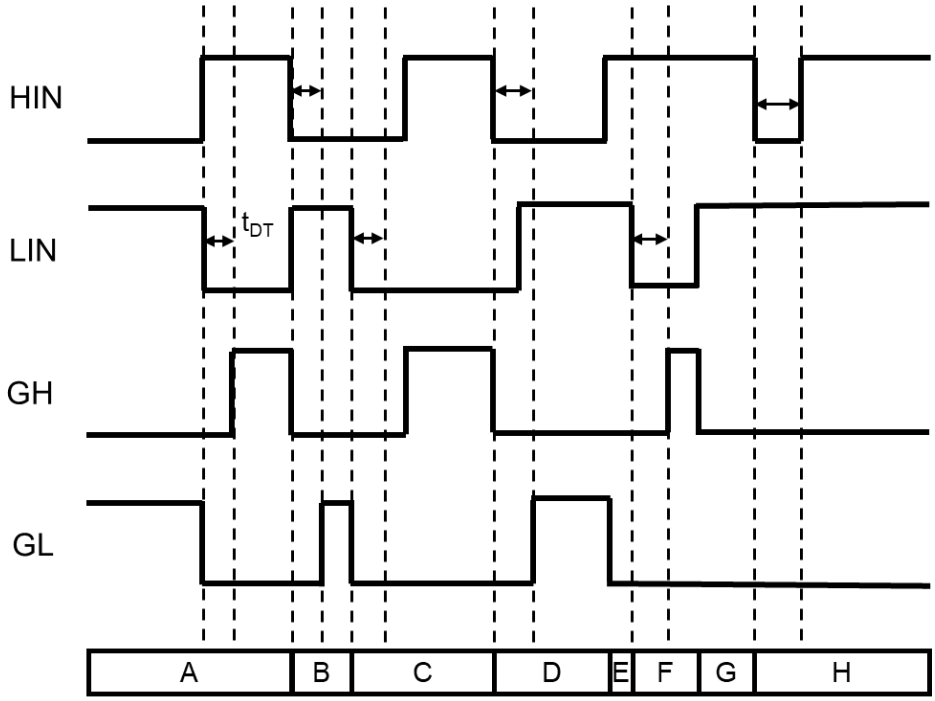


Figure 8.2 Input and Gate Logic with the Programmed Deadtime

Conditions	Results
A: HIN goes high, and LIN goes low.	GL goes low immediately, then GH goes high after the programmed deadtime which is assigned at LIN goes low.
B: HIN goes low, and LIN goes high.	GH goes low immediately, then GL goes high after the programmed deadtime which is assigned at HIN goes low.
C: LIN goes low, then HIN goes high after deadtime.	GL goes low immediately, then GH goes high immediately when HIN goes high.
D: HIN goes low, then LIN goes high before deadtime.	GH goes low immediately, then GL goes high after deadtime.
E: HIN goes high, LIN is still high.	GL goes low immediately, and GH keeps low.
F: HIN is still high, LIN goes low.	GH goes high after deadtime while LIN is low, and GL keeps low.
G: HIN is still high, LIN goes high after deadtime.	GH goes low immediately, and GL keeps low.
H: HIN goes low then goes high before deadtime while LIN is still high.	GH keeps low and GL keeps low because deadtime control.

8.4 Bootstrap structure

A bootstrap circuitry is typically used to supply the high-voltage section. The CGC02002 integrates this structure to reduce the external components.

The Bootstrap integrated circuit is connected to VDD pin and is driven synchronously with the low-side driver.

The use of an external bootstrap diode in parallel to the integrated structure is possible, in particular if the operating frequency is approximately higher than 500 kHz.

9 Typical application diagrams

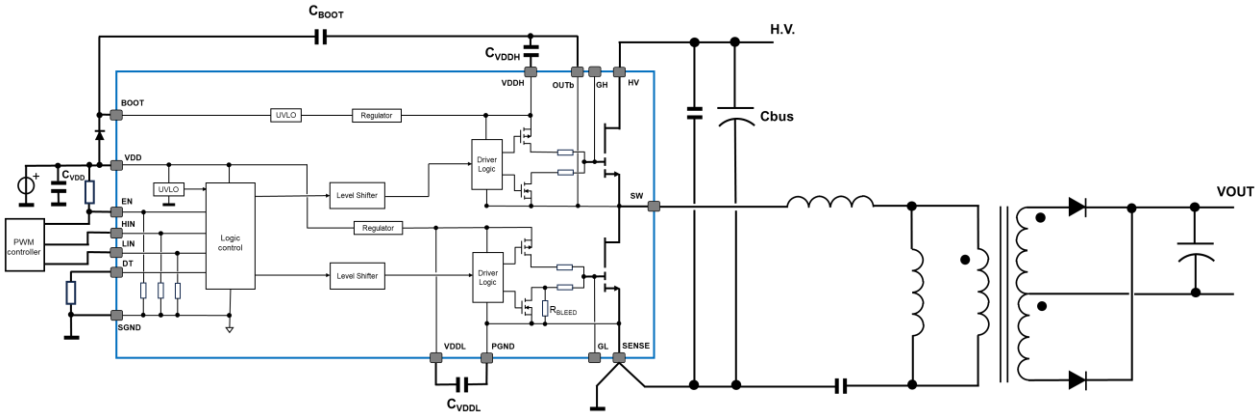


Figure 8.1 Typical application diagram: Resonant LLC converter

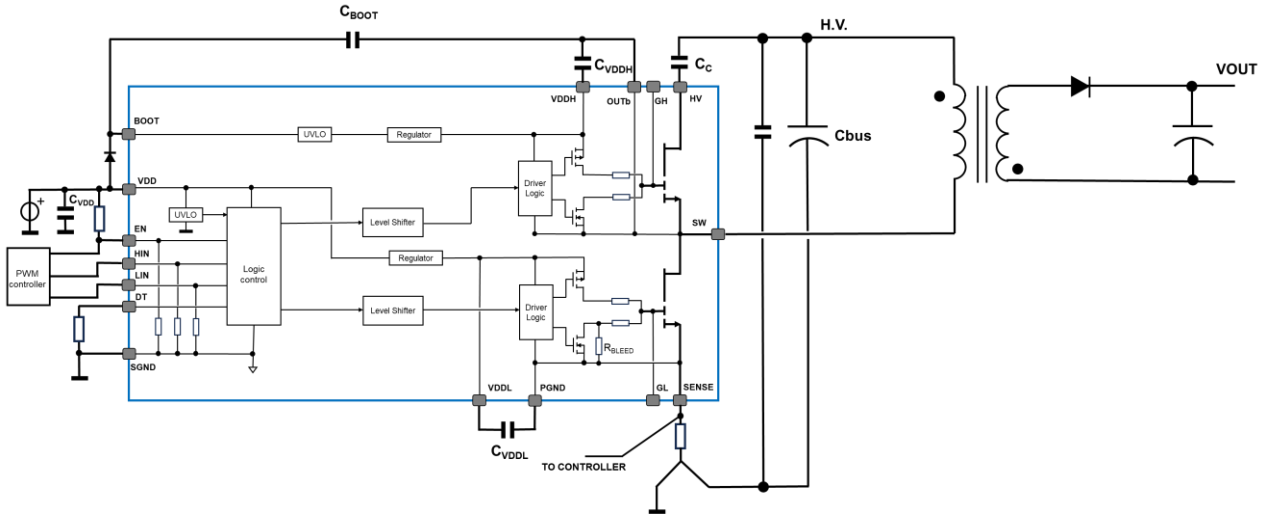
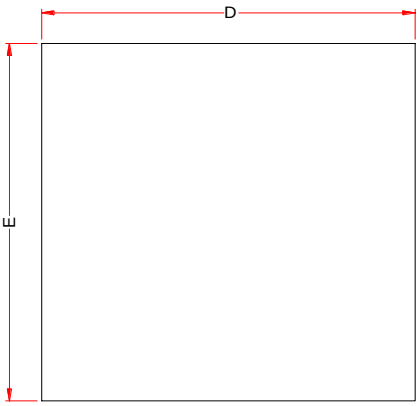
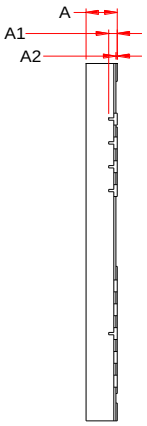


Figure 8.2 Typical application diagram: Active clamp flyback

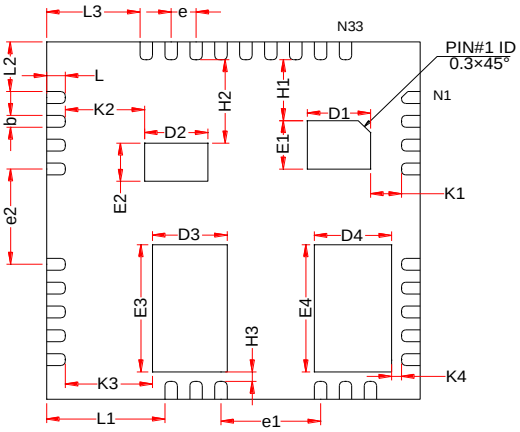
10 Package outlines



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	ASSY lot No.	XXXXXXXX
Row 3	Year & Week	YXWX

	MIN	MID	MAX
A	0.700	0.750	0.800
A1		0.203REF	
A2	0	0.02	0.05
b	0.250	0.300	0.350
D		9.00BSC	
D1	1.425	1.525	1.625
D2	1.425	1.525	1.625
D3	1.700	1.860	1.960
E		9.00BSC	
E1	1.120	1.220	1.320
E2	0.860	0.960	1.060
E3	3.100	3.200	3.300
E4	3.100	3.200	3.300
e		0.600BSC	
e1		2.400BSC	
e2		2.400BSC	
K1	0.644	0.744	0.844
K2	1.810	1.910	2.010
K3	2.000	2.100	2.200
K4	0.140	0.240	0.340
L	0.400	0.450	0.500
L1		2.850REF	
L2		1.250REF	
L3		2.250REF	
H1	1.434	1.534	1.634
H2	2.000	2.100	2.200
H3	0.140	0.240	0.340

11 Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.5	2023-5-5	0.5 version release
1.0	2023-12-5	1.0 version release