CG65012CAD

Description

- GaN enhancement mode power switch
- $R_{DS(on)}$ Typ. 10 mΩ
- Ultra-low FOM
- Simple gate drive requirements (0 V to 6 V)
- Fast and controllable fall and rise times
- Reverse current capability
- Dual gate pads for optimal module layout
- Zero reverse recovery loss

Applications

- On Board Chargers
- Traction Drive
- Bridgeless Totem Pole PFC
- AC-DC Converters
- DC-DC Converters
- Inverters
- Solar Inverters
- Energy Storage Systems
- Uninterruptable Power Supplies
- Industrial Motor Drives

Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS, max}$	650	V
I_D (Note 1)	-	A
$R_{DS(on)}$ (Note 2)	10	mΩ
Die Size	13.29 x 6.32	mm x mm
Die Thickness	300	μm

1) Performance will vary based on assembly technique and substrate of choice

2) Defined by chip design. Die is not tested to full current in production.

Absolute Maximum Ratings (TSUBSTRATE = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain to Source Voltage (Note 3)	$V_{DS(transient)}$	850	V
Gate-to-Source Voltage	V_{GS}	-5 to +7	V
Gate-to-Source Voltage - transient (Note 3)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current T_{SUB} = 25 °C (Note 4)	I_{DS}	-	A

3) For < 100 μs

4) Performance will vary based on assembly technique and substrate of choice

Table 2 Ordering Information

Part number	Ordering code	Packing method
CG65012CAD	CG65012CAD	

Electrical Characteristics at Wafer Level

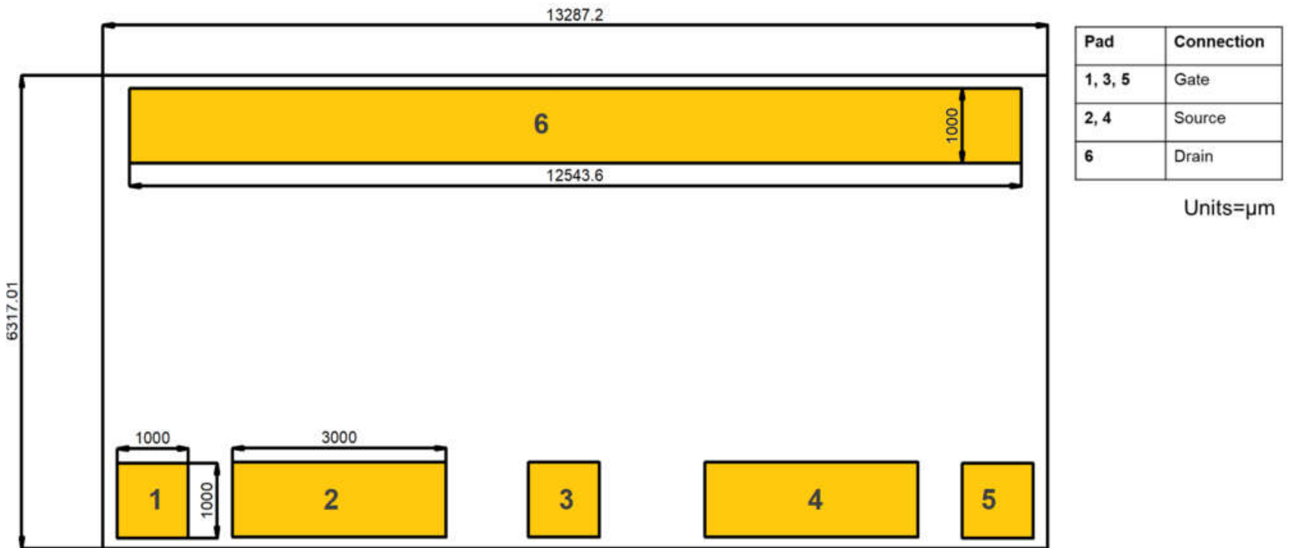
Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-source voltage	$V_{DS, max}$	650			V	V_{GS} =0 V, I_{DSS} < 100 μA
Drain-to-Source on-state resistance (Note 5)	$R_{DS(on)}$		10	12	mΩ	V_{GS} = 6 V, T_J = 25°C, I_{DS} = 20 A
			25			V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 20 A
Gate threshold voltage	$V_{GS(TH)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_D = 30 mA
Drain-to-Source leakage current	I_{DSS}		2		μA	V_{DS} = 650 V, V_{GS} = 0 V
Gate-to-Source leakage current	I_{GSS}		150		μA	V_{GS} = 6 V, V_{DS} = 0 V
Input capacitance	C_{iss}		1000		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output capacitance	C_{oss}		256		pF	
Reverse transfer capacitance	C_{rss}		3		pF	
Gate charge	Q_G		28		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		7.6		nC	
Gate-to-Drain Charge	Q_{GD}		8		nC	
Output charge	Q_{OSS}		255		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse recovery charge	Q_{RR}		0		nC	

5) Defined by chip design. Die is not tested to full current in production.

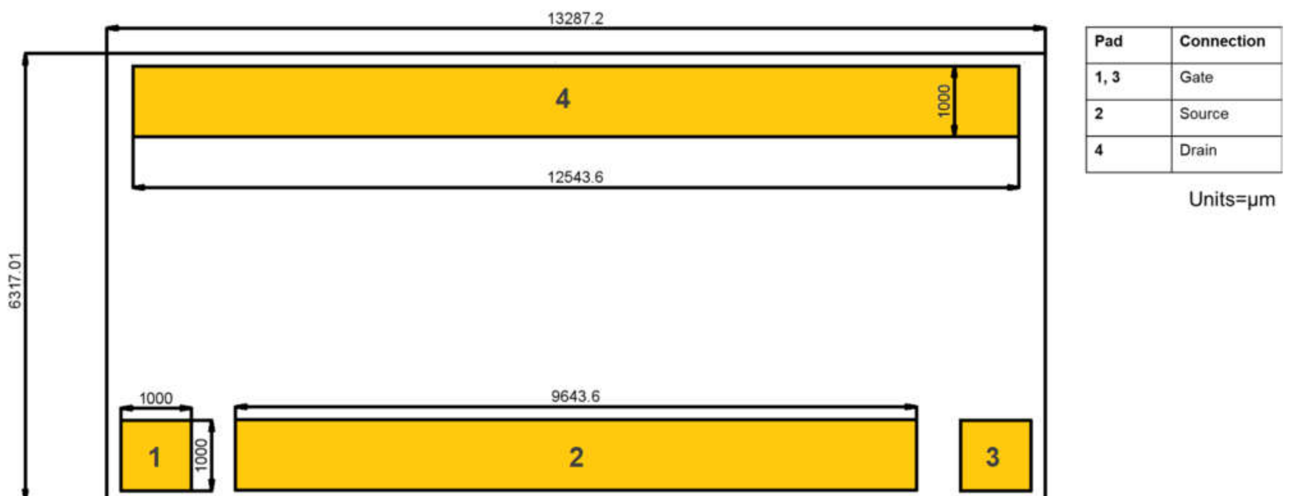
Dimensions

There are two Die Bonding Pad Drawing as below.



Pad	Connection
1, 3, 5	Gate
2, 4	Source
6	Drain

Figure 1 Die Bonding Pad Drawing-1 (Split Source)



Pad	Connection
1, 3	Gate
2	Source
4	Drain

Figure 2 Die Bonding Pad Drawing-2

Top pad is metallized by Cu/Ni/Au with thickness of 10/3/1 μm.
Backside metallization is Al/Ti/NiV/Au with thickness of 0.2/0.1/0.35/0.1 μm.