

杭州云镓半导体科技有限公司
Hangzhou CloudSemi Technology Co., Ltd

A Basic Introduction to GaN

GaN Device R&D Team

Powering the Dreams!



CLOUDSEMI
云镓半导体

CONTENTS

- 1. What is GaN device?**
- 2. How does GaN work?**
- 3. How to drive GaN?**
- 4. About us**

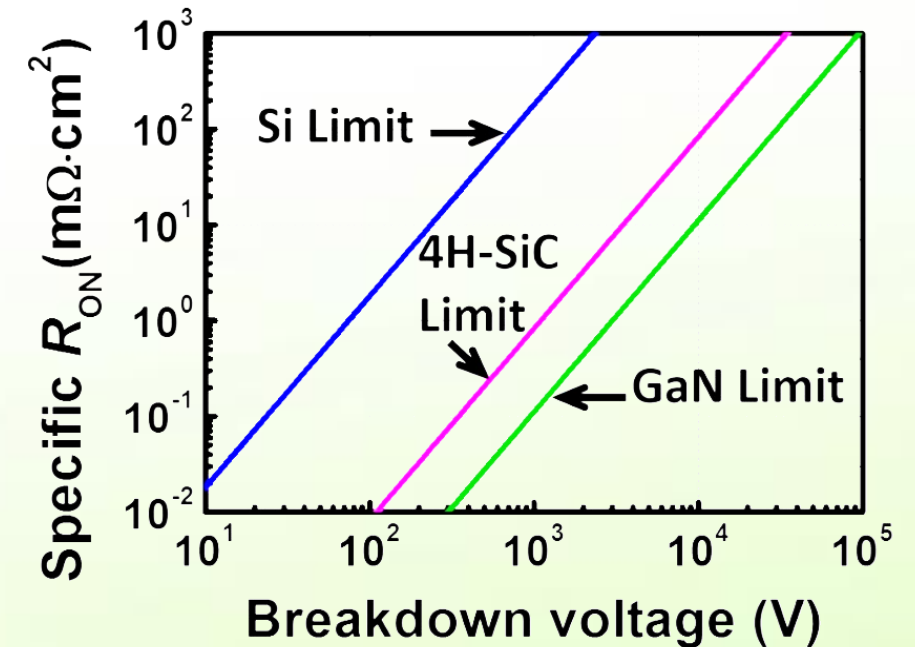
PART 01

What is GaN device?

www.cloudsemi.net

Gallium Nitride: superior material properties

Parameters	Units	Si	GaAs	4H-SiC	GaN
Energy bandgap (E_g)	eV	1.12 (Indirect)	1.42 (Direct)	3.3 (Indirect)	3.4 (Direct)
Thermal conductivity (Θ)	W/cm·K	1.5	0.5	4.5	1.3
Dielectric constant (k)	N.A.	11.8	13.1	10	9.0
Electron mobility (μ_n)	cm ² /(V·s)	1350	8500 (2DEG)	720	900 (bulk) ~2000 (2DEG)
Critical electric field (E_C)	MV/cm	0.3	0.4	2.0	3.3
Saturation velocity of electrons (V_{sat})	10 ⁷ cm/s	1.0	2.0	2.0	2.5
CFOM ($k\Theta\mu_n V_{sat} E_C^2$)	Normalized to Si	1	8	121	296 (2DEG)



The direct bandgap → suitable for LED application

High electron mobility → competitive as RF devices in 5G era

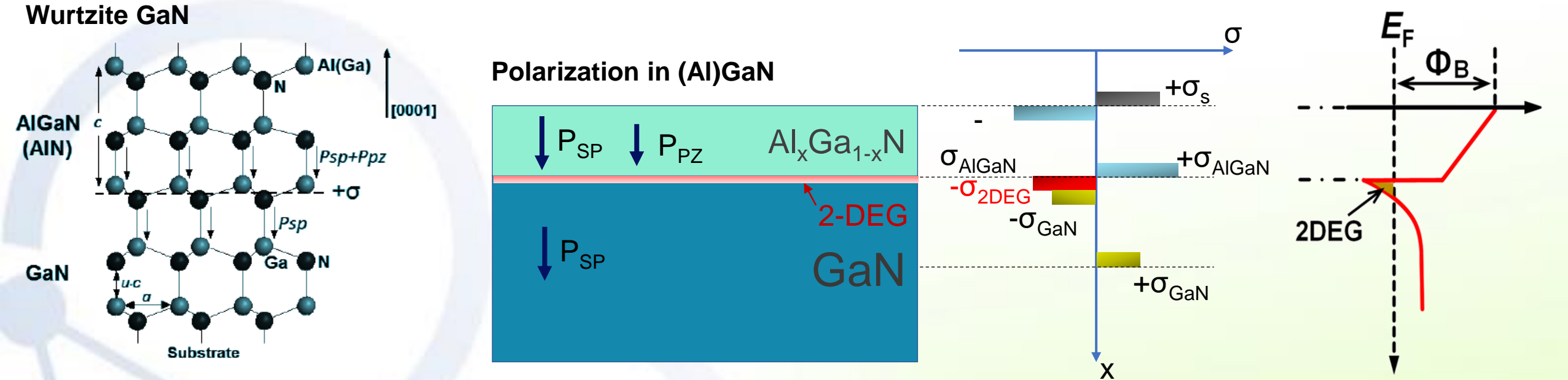
Wide energy bandgap → High operating temperature

High critical E-field → High voltage blocking capability

High electron mobility → High switching frequency

Superior material properties for power devices

AlGaN/GaN heterojunction

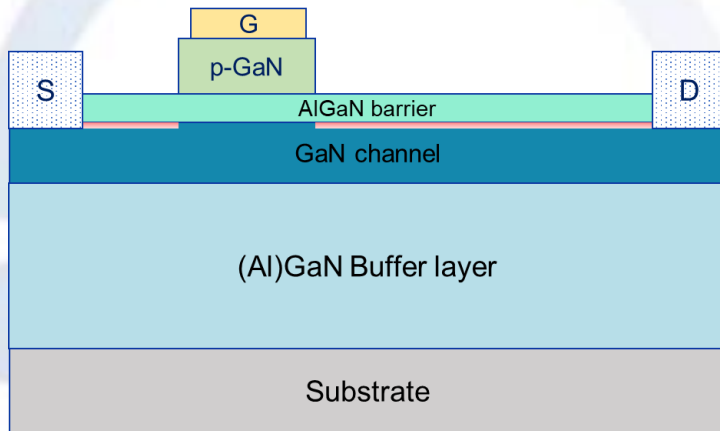


- Spontaneous & piezoelectric polarization effect in AlGaN/GaN
 - Surface state ionization → electron formation at material interface
 - Confined quantum well → two-dimension electron gas (2-DEG)
- ➔ Doping-free process, junction-less structure → **ZERO Q_{rr} !**
- ➔ Innate conductive channel → **How to realize normally-OFF device (i.e. enhancement mode, E-mode)?**
- High Electron Mobility Transistor (HEMT)**

Normally-OFF-operation GaN devices

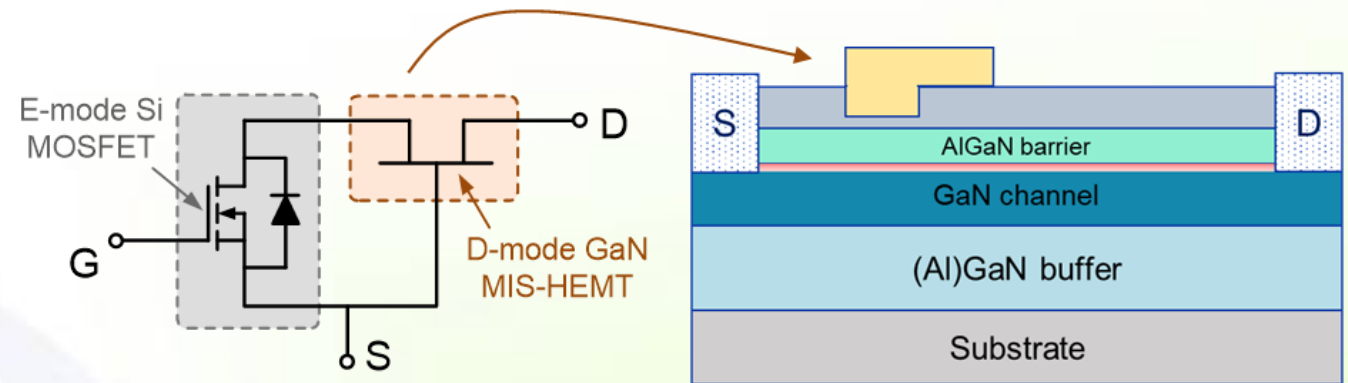
Mainstream methods to normally-OFF device

p-GaN gate technology (CloudSemi)



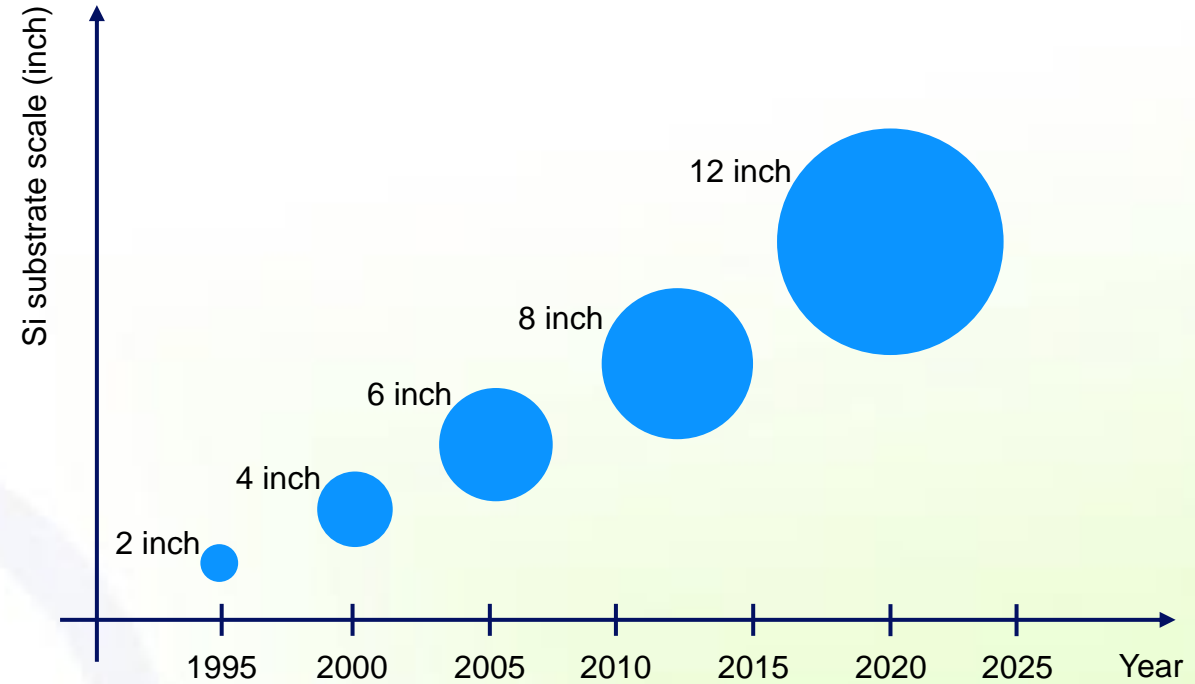
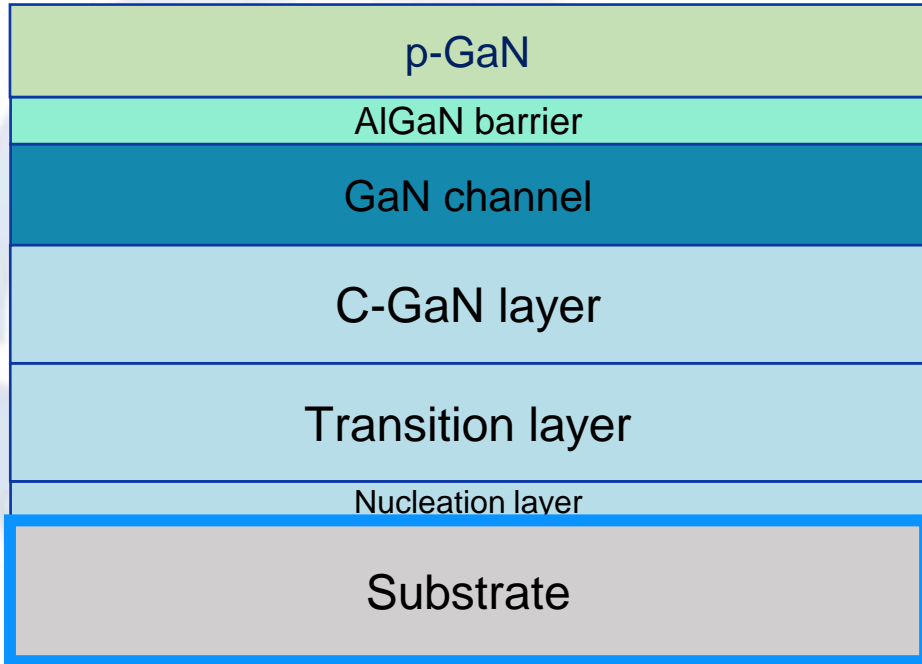
- Selective p-GaN to deplete channel in gate region
- Single-chip scheme
- A simple 3-terminal device
- High switching frequency
- Easy to parallel multi devices
- Easy to form driver/protection/sensing/etc. integration
- Suitable for low-voltage and high-voltage devices

Cascode technology



- Series of E-mode Si MOS to achieve normally-OFF
- Multi-chip scheme (needs an additional resistor)
- Existing risks of balancing Si and GaN static/dynamic behavior
- Limited switching frequency by Si MOS
- Difficult to parallel
- Cannot form monolithic ICs
- Only competitive in high-voltage devices

How to form a GaN device: substrate choices

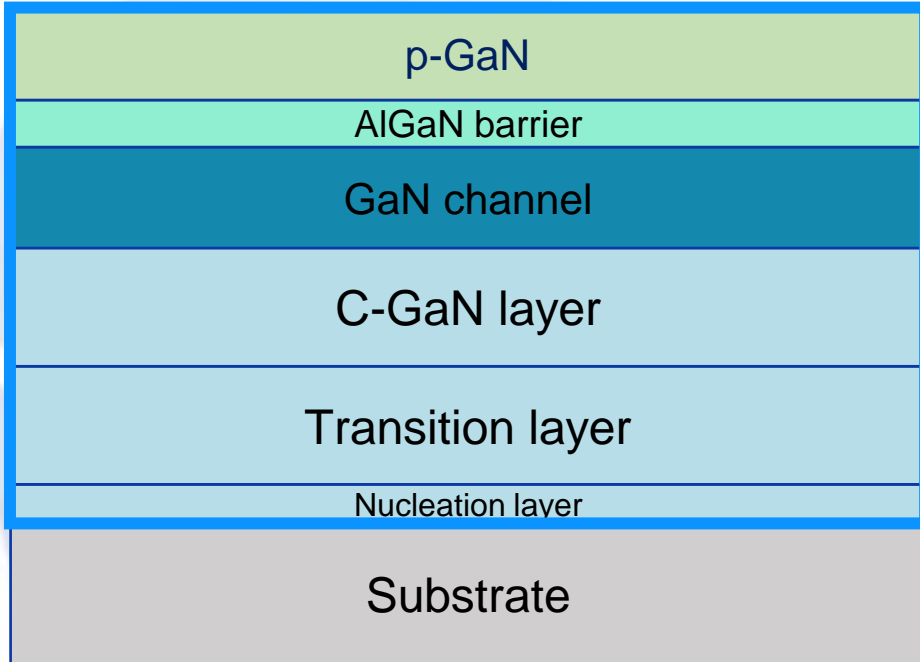


Materials	Substrate Cost	Wafer Size	Applications
GaN	> 100X	2/4 inch	Power
SiC	~50X	4/6 inch	RF, Power
Al ₂ O ₃	~10X	4/6 inch	LED, Power
Silicon	1X	6/8/12 inch	LED, RF, Power

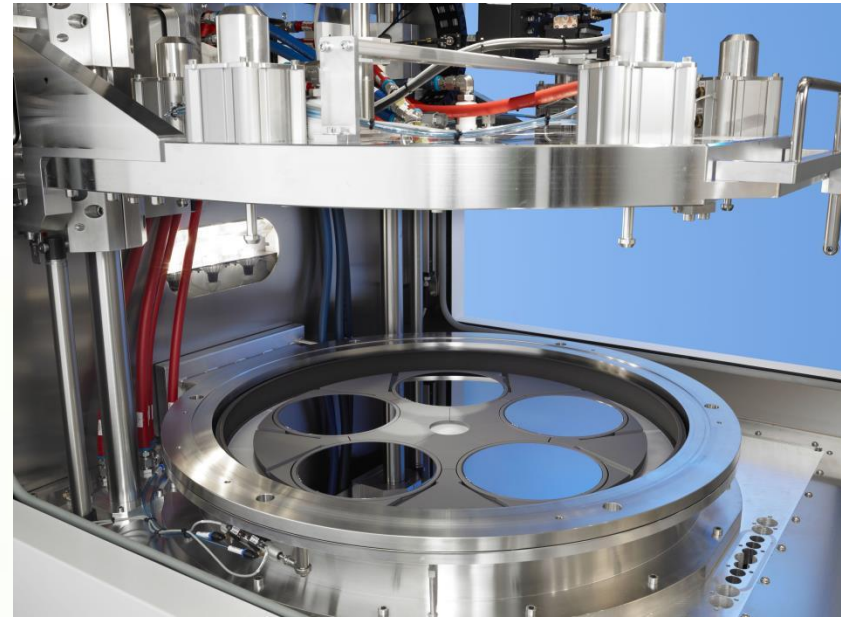
Choosing silicon as substrate materials:

- Low material cost
- Scaling up on wafer size (up to 12 inch)
- Compatible to traditional CMOS process

How to form a GaN device: epi-layer growth



MOCVD reactor



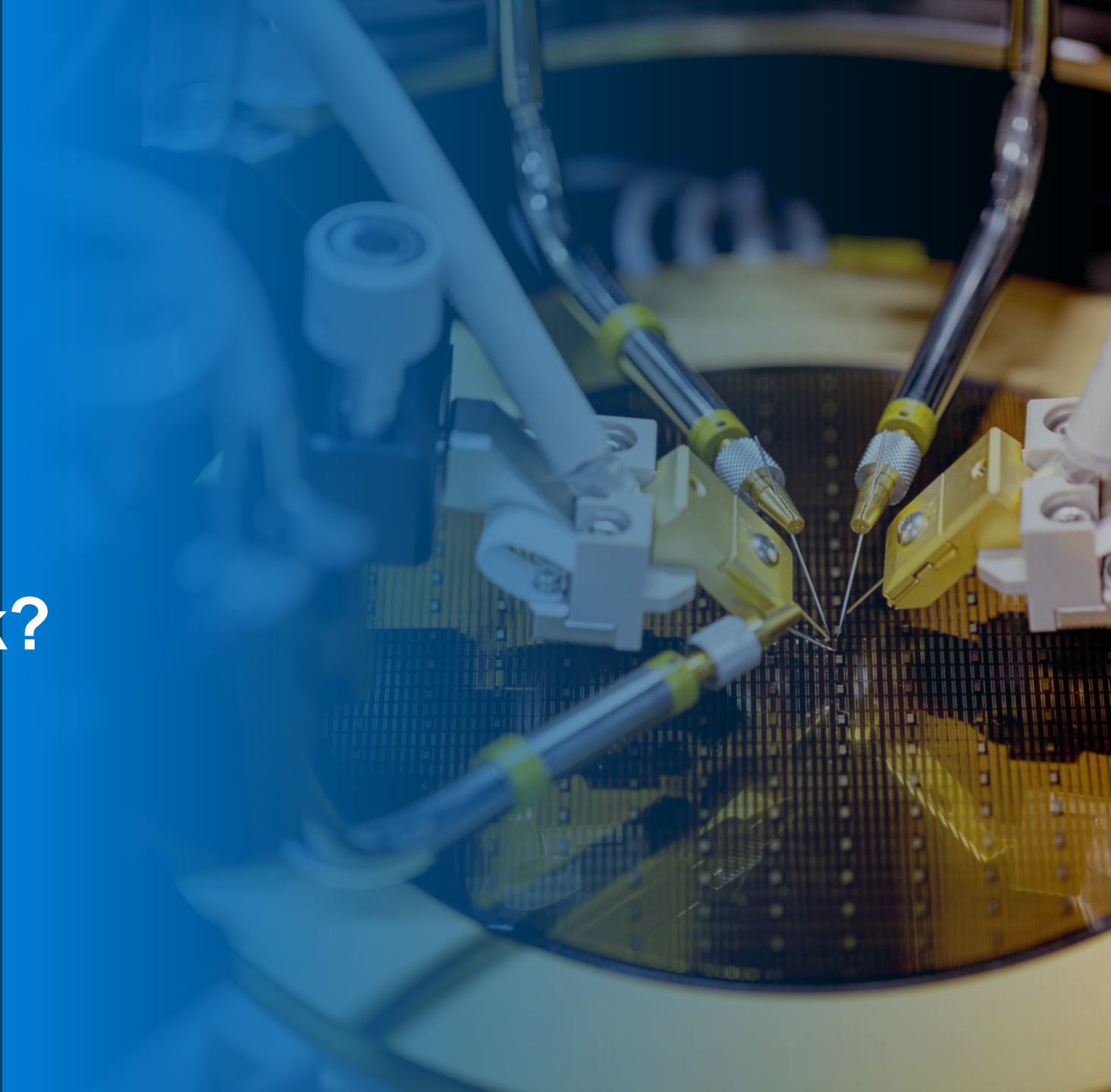
Cite from <http://uef.fei.stuba.sk/moodle/mod/book/print.php?id=7920&chapterid=141>

- Only several-micrometer epilayer on the substrate, low material cost.
- Epilayer structures strongly determine the device rating and performance.
- **Metal-Organic-Chemical-Vapor-Deposition (MOCVD)** method is commonly used.
- **Lattice and thermal expansivity mismatch** among the materials make the growth need well controlled.

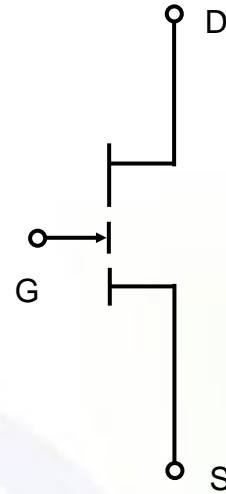
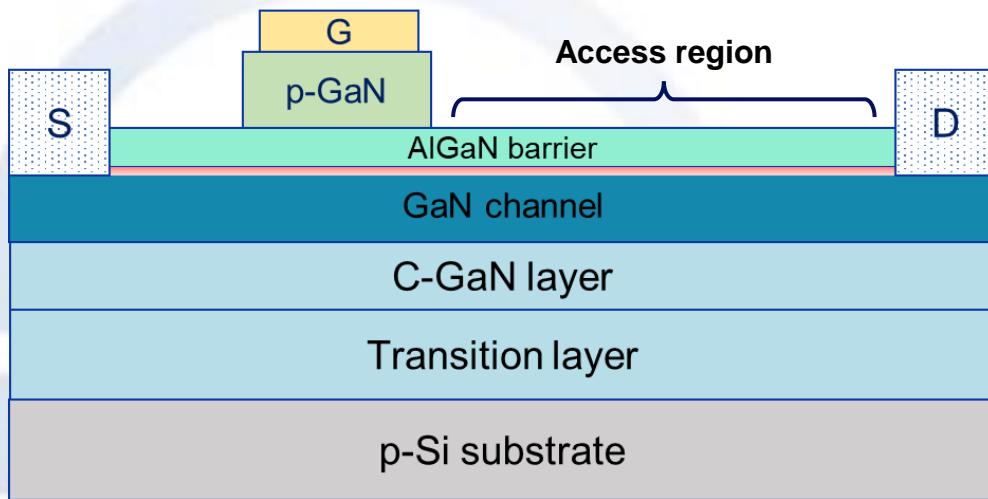
PART 02

How does GaN work?

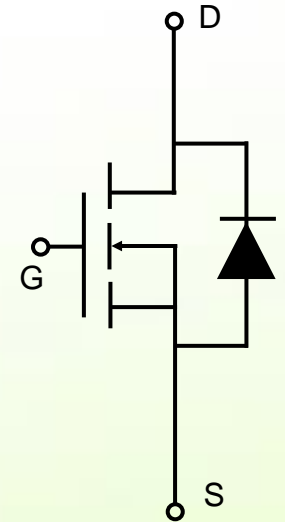
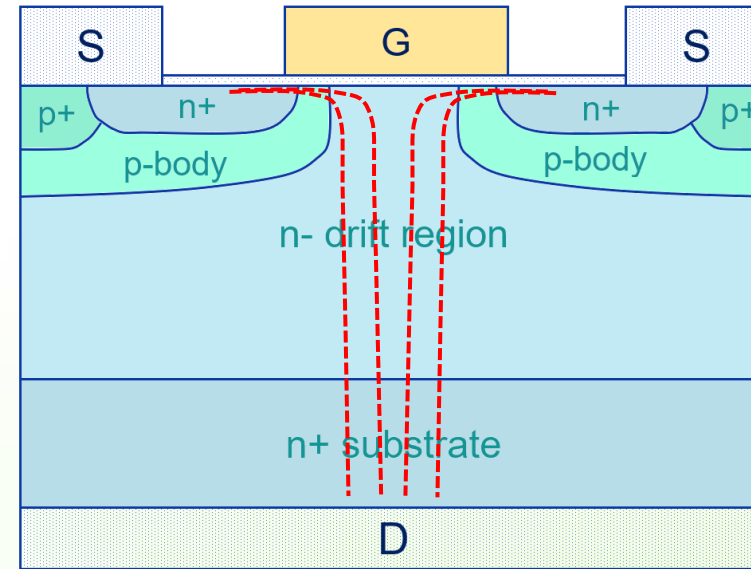
www.cloudsemi.net



Device structures: lateral GaN vs vertical Si

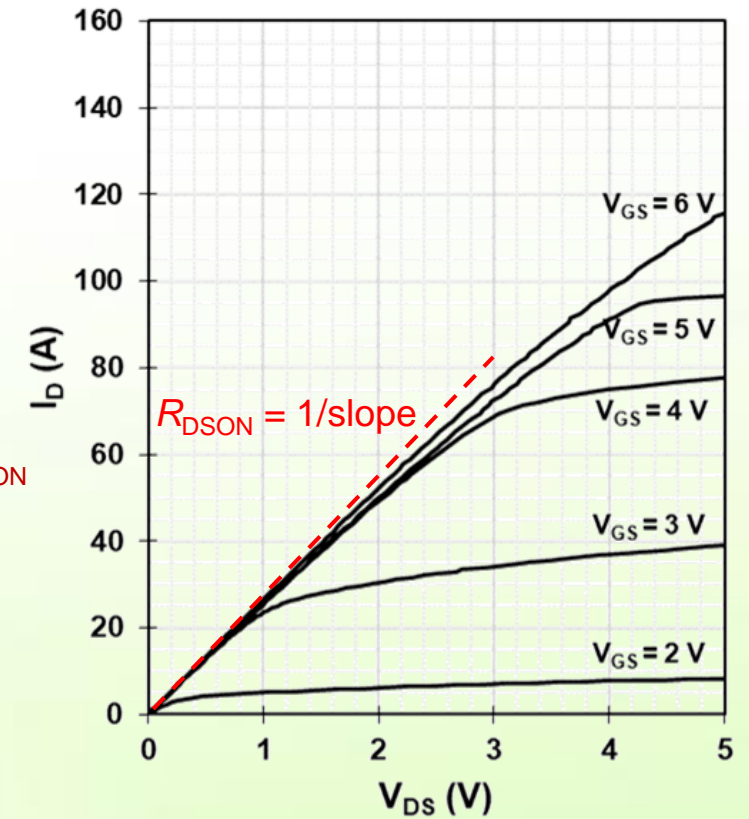
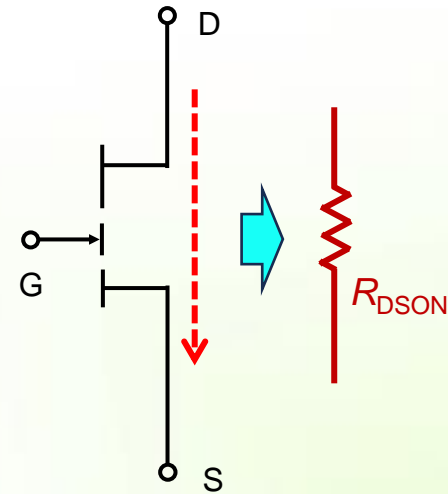
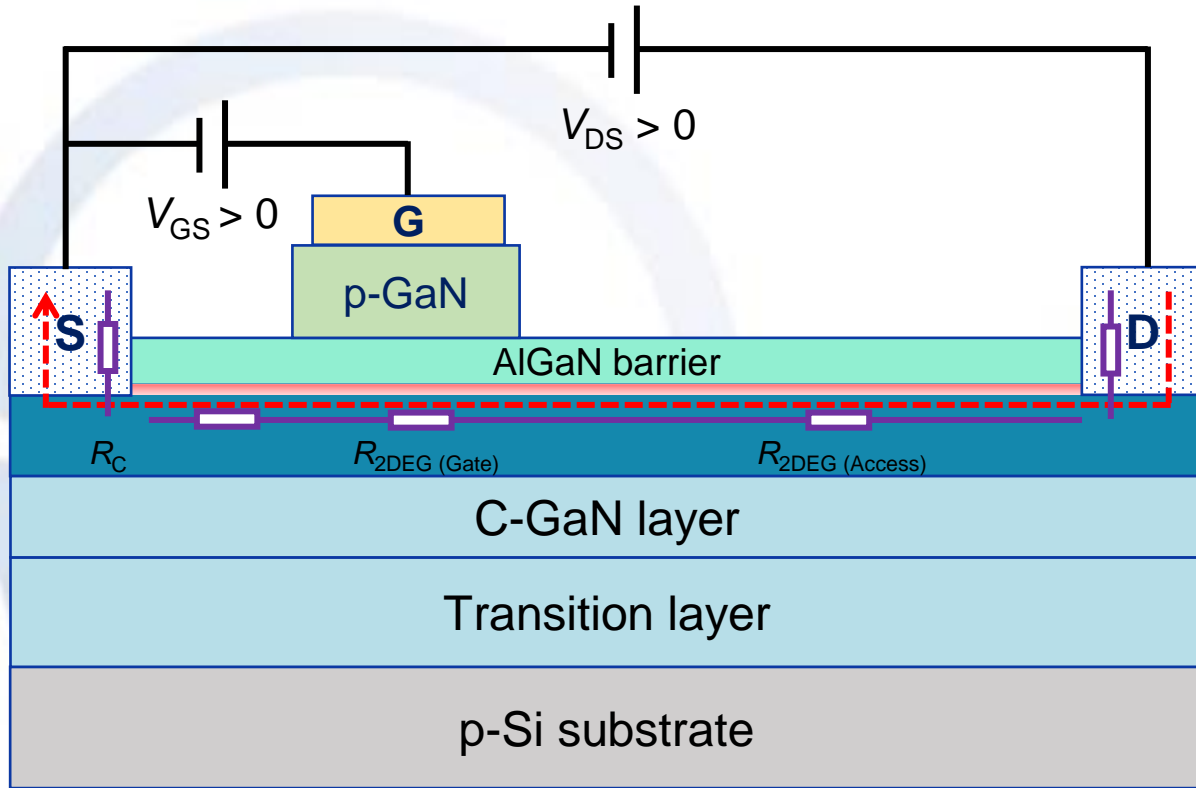


- Three terminals (S/G/D) are on the top
- P-type Si Sub should be electrically connected to Source
- Doping free, PN-junction-less, **no body diode**
- **Lateral** conductive channel
- **Access region** design determines HV static/dynamic behaviors
- Metal-semiconductor (**MS**) structure to form Gate
- Voltage-driven method



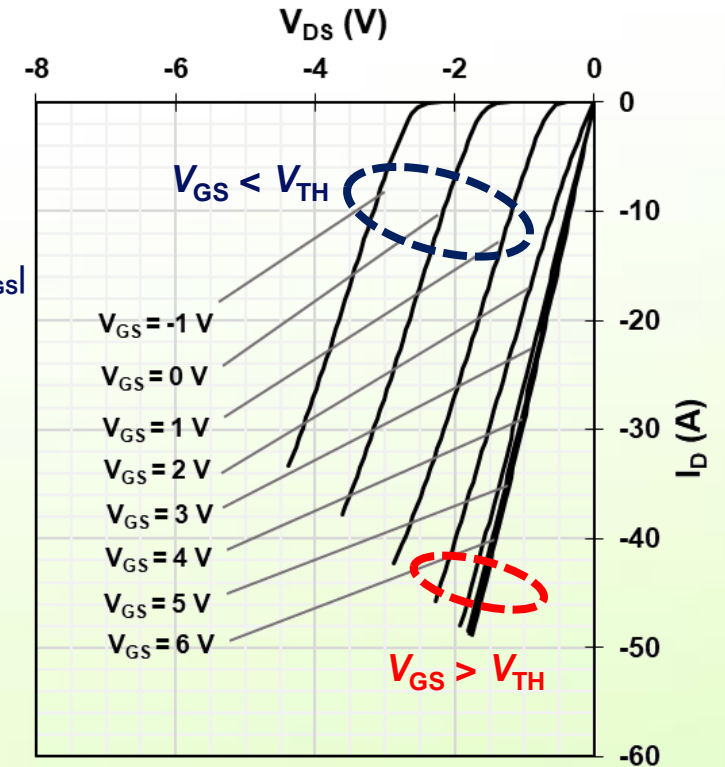
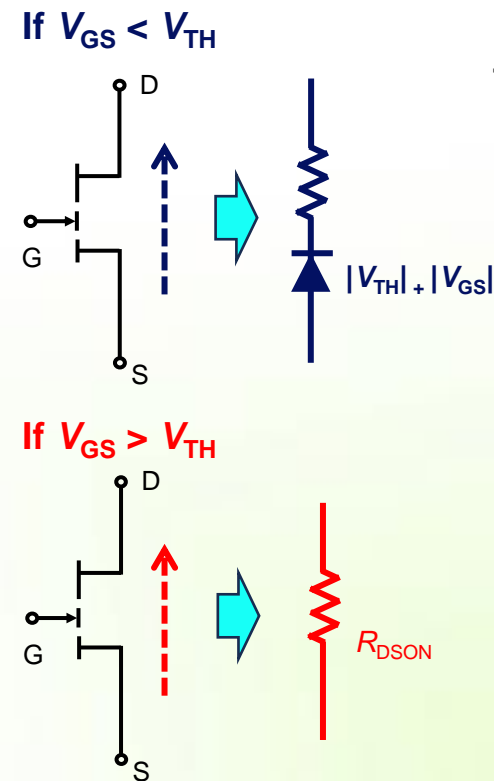
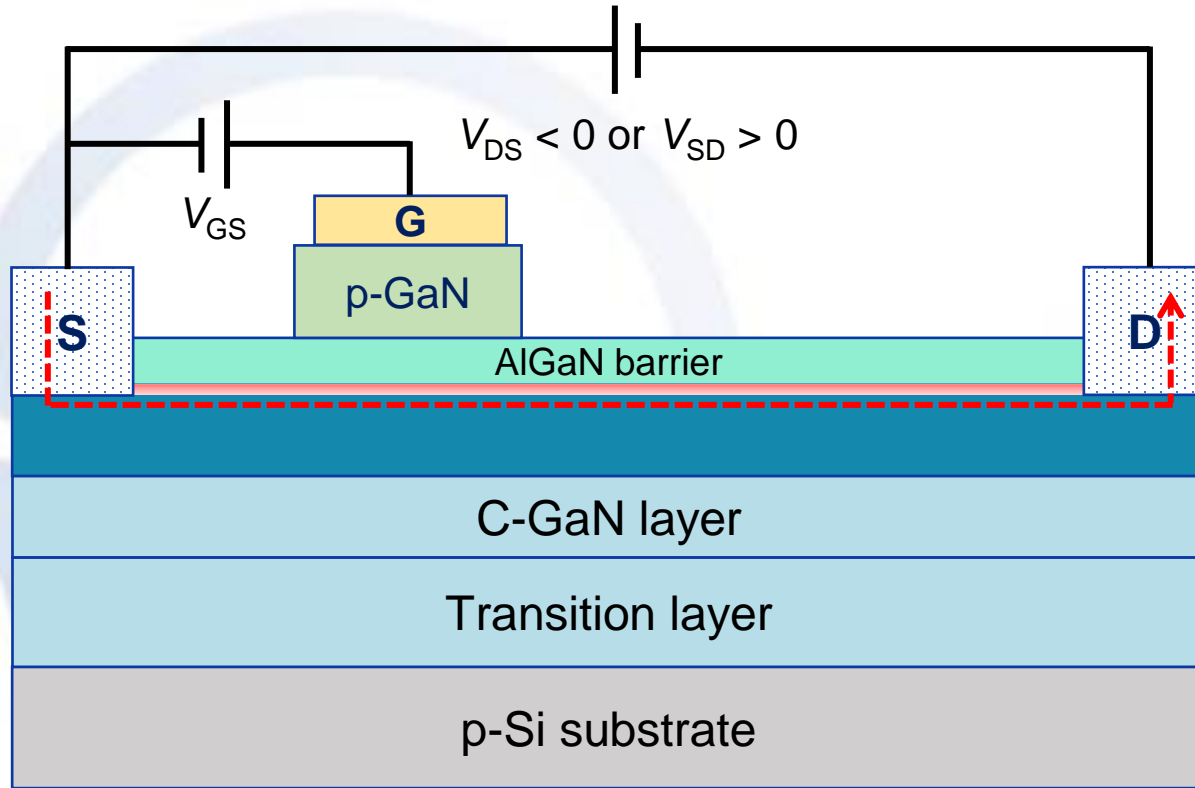
- Gate & Source are on the top, and Drain is bottom
- Low-resistivity n+ Si sub is as drain terminal
- Doping process to form PN junctions, **with body diode**
- **Vertical** conductive channel
- **Drift region** design determines HV behaviors
- Metal-oxide-semiconductor (**MOS**) structure to form Gate
- Voltage-driven method

Forward conduction



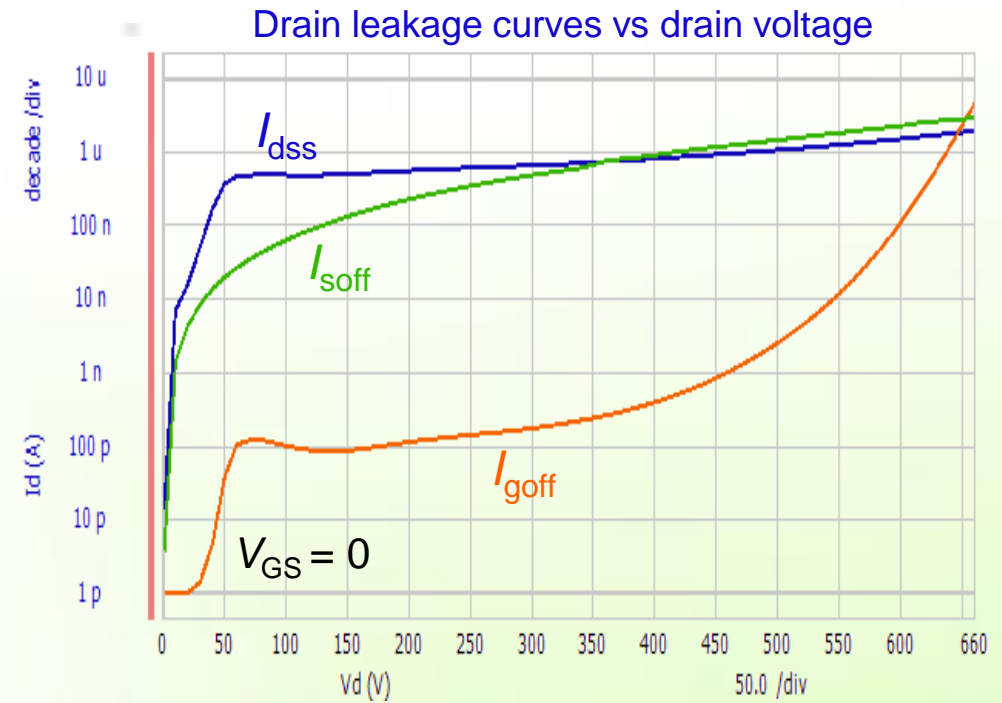
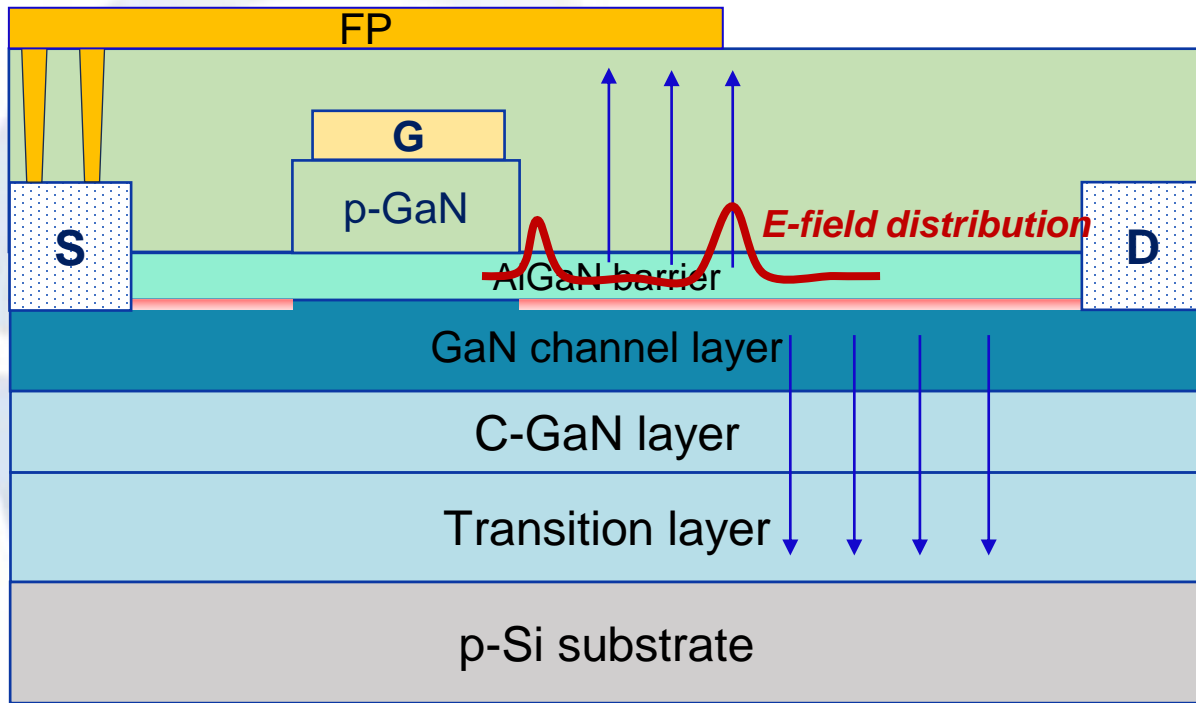
- Forward conduction mode: similar to a traditional MOSFET behavior.
- As V_{GS} exceeds the threshold voltage V_{th} , the channel forms beneath the gate region.
- The drive voltage V_{GS} directly controls the device on-state resistance R_{DSON} .
- Front-end R_{DSON} consists of contact res. R_C , 2-DEG res. underneath the Gate, and 2DEG res. in the access region.

Reverse conduction



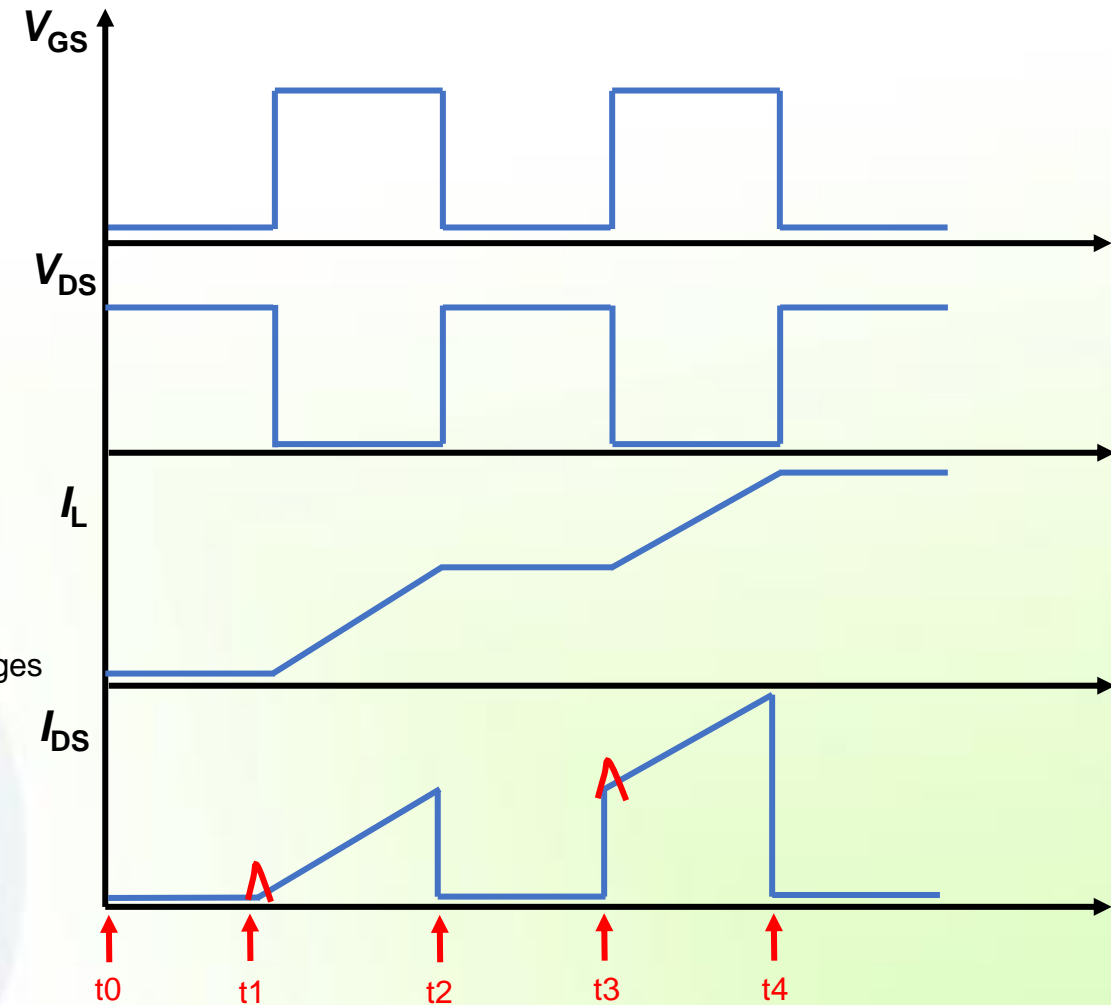
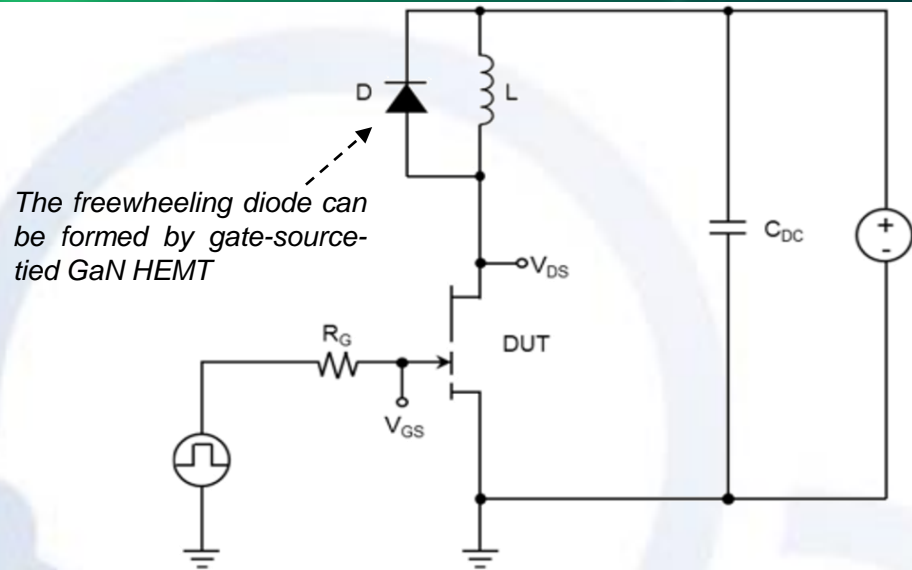
- **Reverse conduction mode:** a little different to traditional Si MOSFET because of the lack of body diode.
- If $V_{GS} < V_{TH}$, current can only flow through the channel as V_{GD} exceeds the V_{TH} , i.e. $V_{SD} > |V_{TH}| + |V_{GS}|$
- If $V_{GS} > V_{TH}$, the reverse conduction behavior is similar to the forward mode.
- Lack of body diode delivers **Zero Q_{rr}** but **a little higher deadtime loss**. Designers can optimize $V_{GS,OFF}$ and deadtime duration.

OFF-state blocking capability



- OFF-state: the behavior is similar to a traditional MOSFET.
- The high-voltage drain terminal generates high E-field toward the gate edge. The field plate (FP) can help to modulate the surface E-field distribution.
- The buffer layer should feature high quality in order to stand the high voltage drop from the drain to substrate.
- Total drain leakage current I_{dss} consists of gate leakage I_{loff} , and source leakage I_{soff} (including substrate leakage).

GaN switching behaviors



A double pulse tester can be used to evaluate GaN device switching behaviors:

- **t0~t1, high voltage soak duration.** GaN is biased under HV OFF-state.
- **t1, zero-current turn-on transient.** Freewheeling diode's capacitance C_D discharges through GaN channel, simultaneously with GaN device's output capacitance C_{oss} .
- **t1~t2, GaN is turned on.** HV DC charges inductor through GaN channel.
- **t2, HSW turn-off transient.** Load current then charges GaN C_{oss} and diode capacitance C_D .
- **t2~t3, freewheeling mode.** GaN is biased under HV OFF-state.
- **t3, HSW turn-on transient.** Load current of inductor, and discharge current of freewheeling diode C_D and GaN C_{oss} , flow through the GaN channel.
- **t3~t4, GaN device is turned on.** HV DC charges inductor through GaN channel again.
- **t4, HSW turn-off transient.**

* Detailed introduction to switching behaviors refer to Application Note page on www.cloudsemi.net.

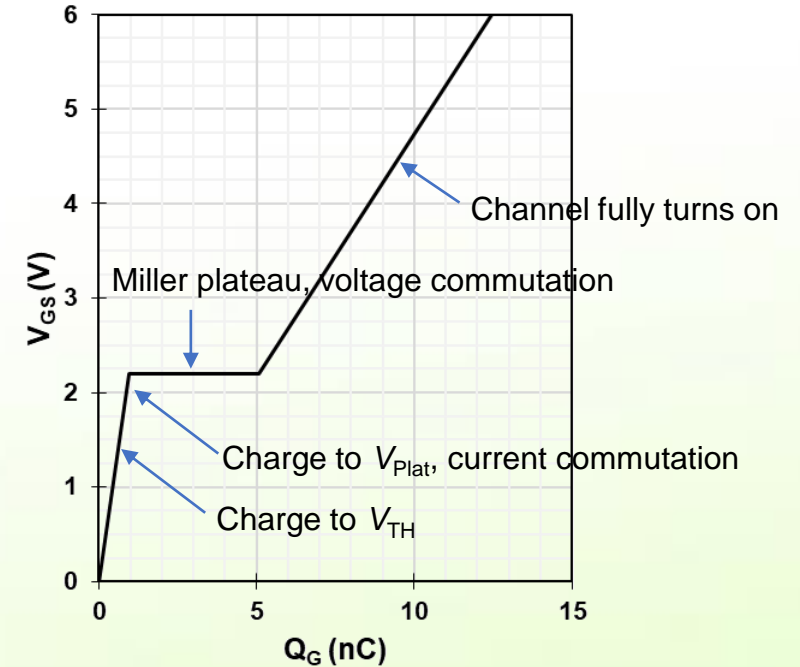
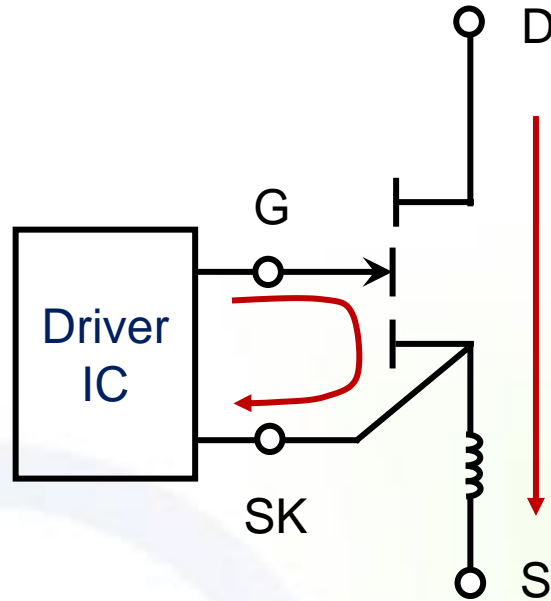
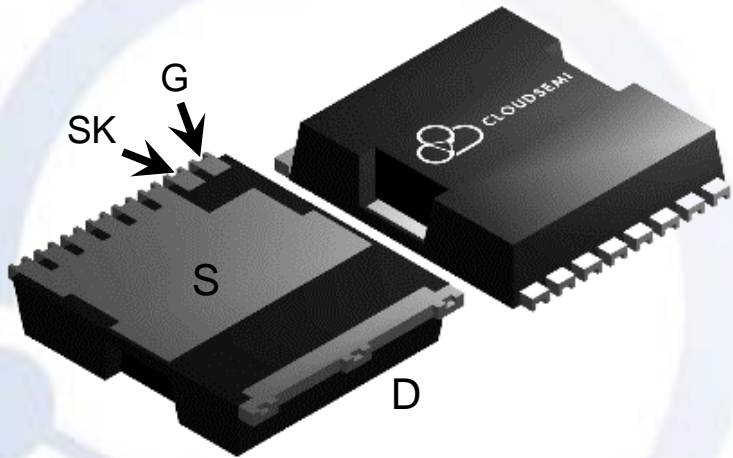
PART 03

How to drive GaN?

www.cloudsemi.net



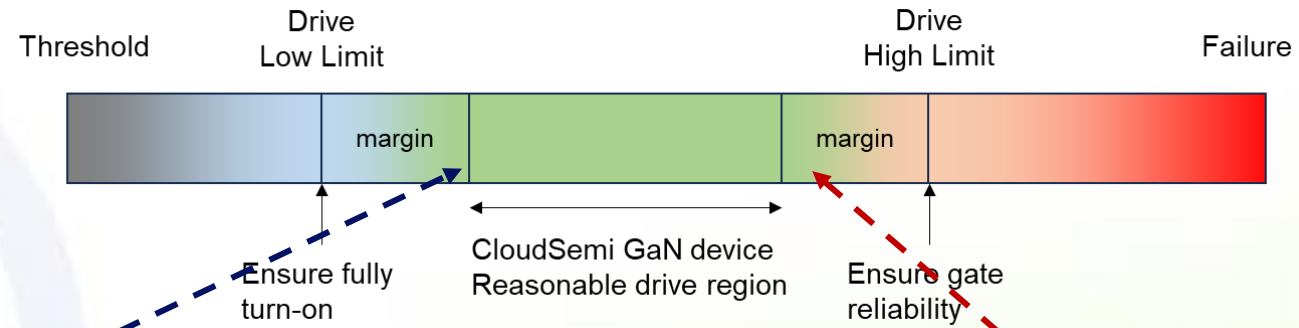
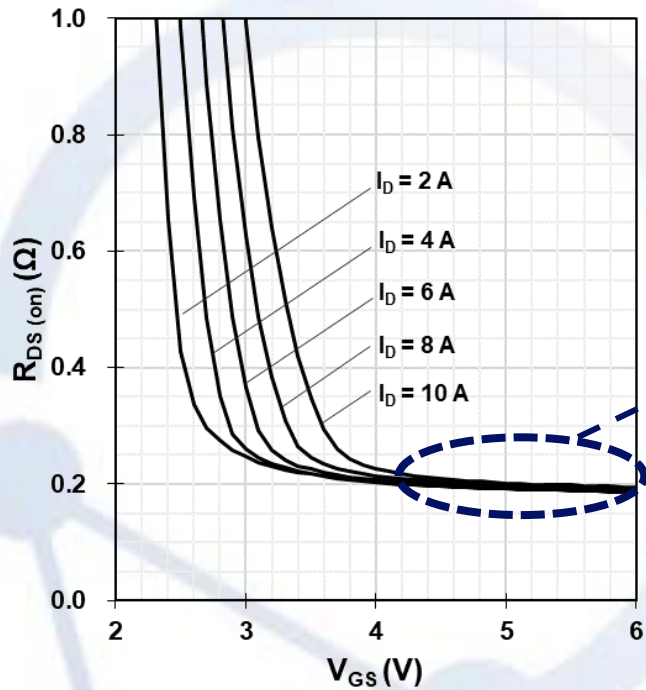
Easy to drive a GaN device



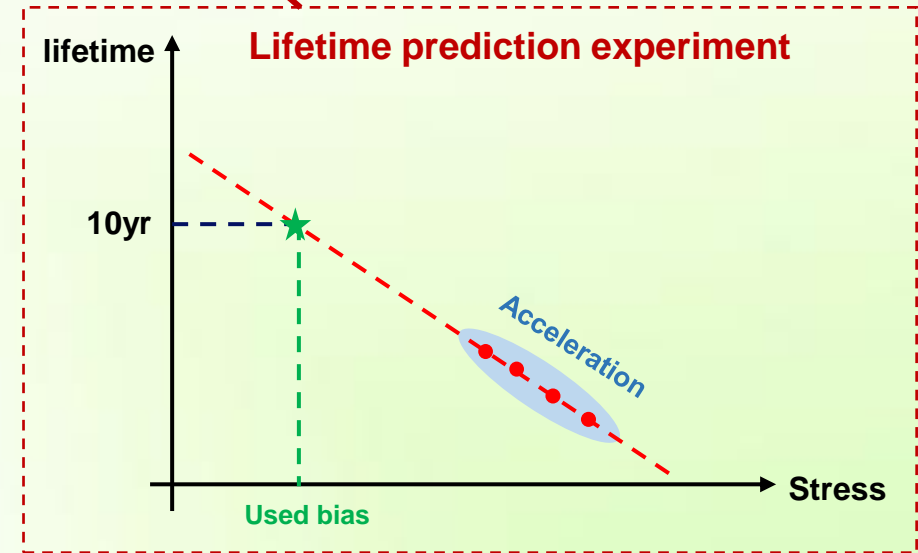
- CloudSemi's GaN is a voltage-driven power device. The driving scheme is similar to MOSFET device by charging and discharging C_{ISS} .
- Simple slew rate control by adjusting R_G in the driving loop.
- Much lower $R_{DSON} * Q_G$, then much faster switching speed.
- Low threshold voltage ($\sim 1.5V$) should be carefully considered during circuit design.
- Gate drive voltage should be well chosen, according to gate performance.

* Detailed introduction to switching behaviors refer to Application Note page on www.cloudsemi.net.

How to choose gate drive voltage?

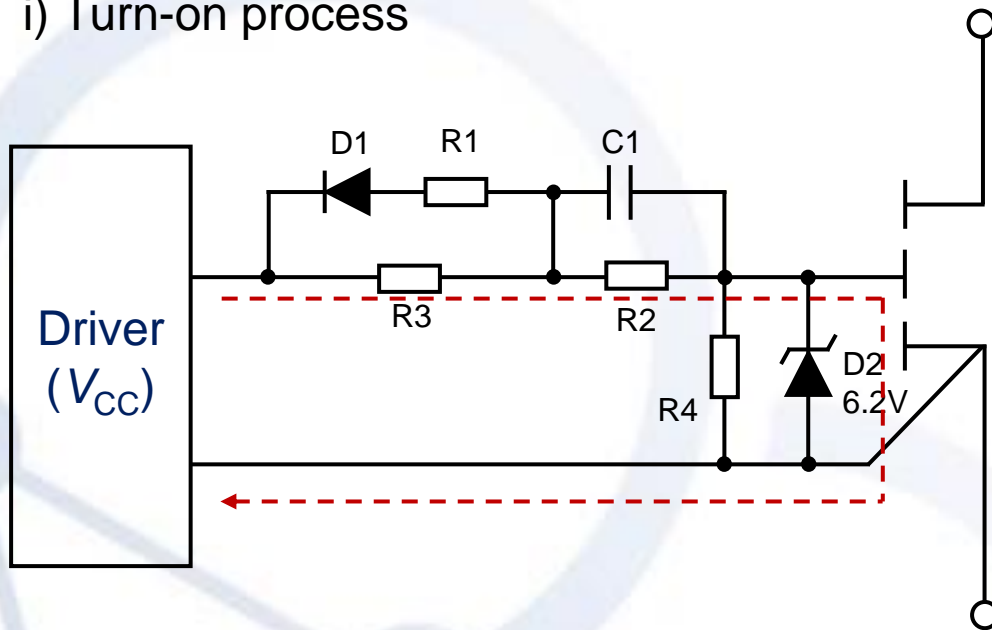


- GaN gate drive voltage should be well chosen according to design platform.
- The **low-limit** of drive voltage should make sure device is fully turned on.
- The **high-limit** of drive voltage should ensure a long-term reliability to meet the lifetime requirement.
- Additional margin is needed in case of the driver instability.

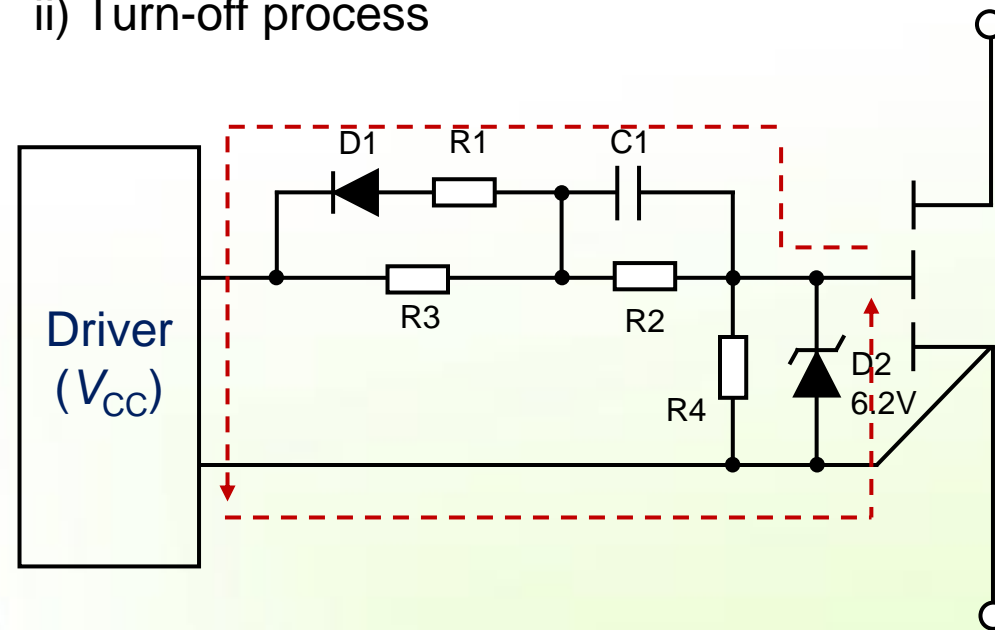


How to use a Si driver to drive GaN?

i) Turn-on process



ii) Turn-off process

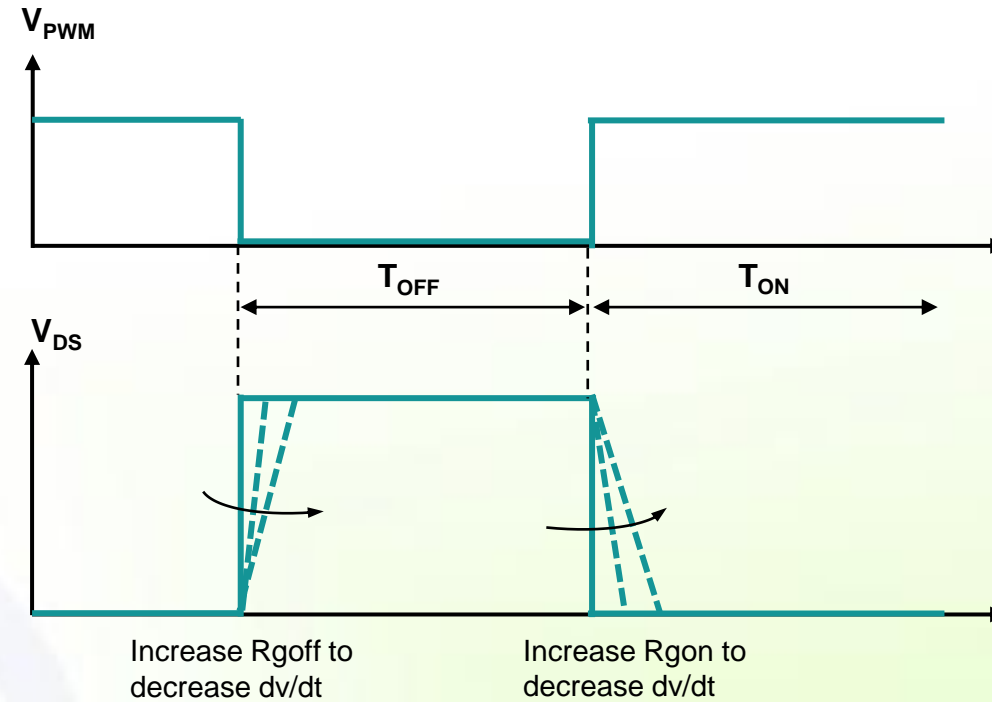
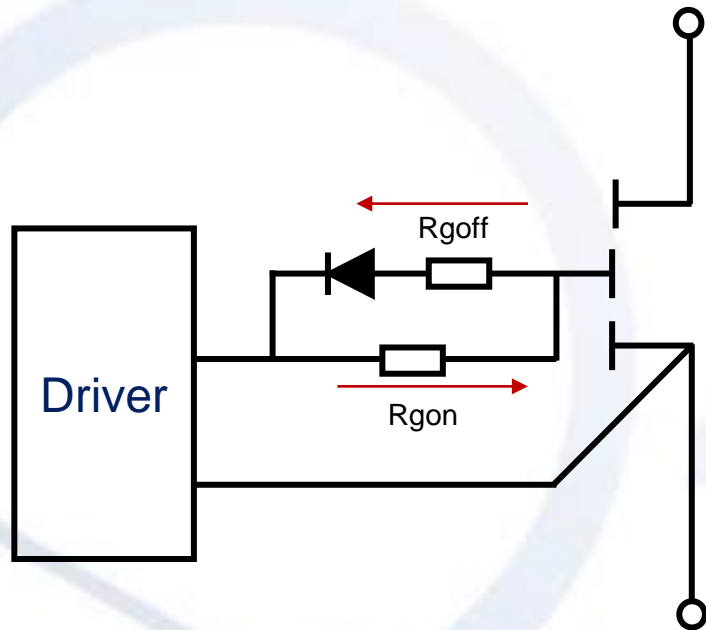


Customers can use a traditional Si driver to drive GaN devices as above:

i) Turn-on process: the driving current path is '*driver-R3-R2-R4//D2-GND*'. The paralleled 6.2V Zener diode can provide with a safe drive voltage. Here, the voltage drop across C1 is $V_{C1} = V_{CC} - 6.2V$.

ii) Turn-off process: capacitor C1 discharges through the path of '*R1-D1-driver-GND*'. Benefiting from the C1, the gate-to-source voltage will feature a transient negative overshoot, avoiding the false turn-on.

How to control slew rate of GaN?

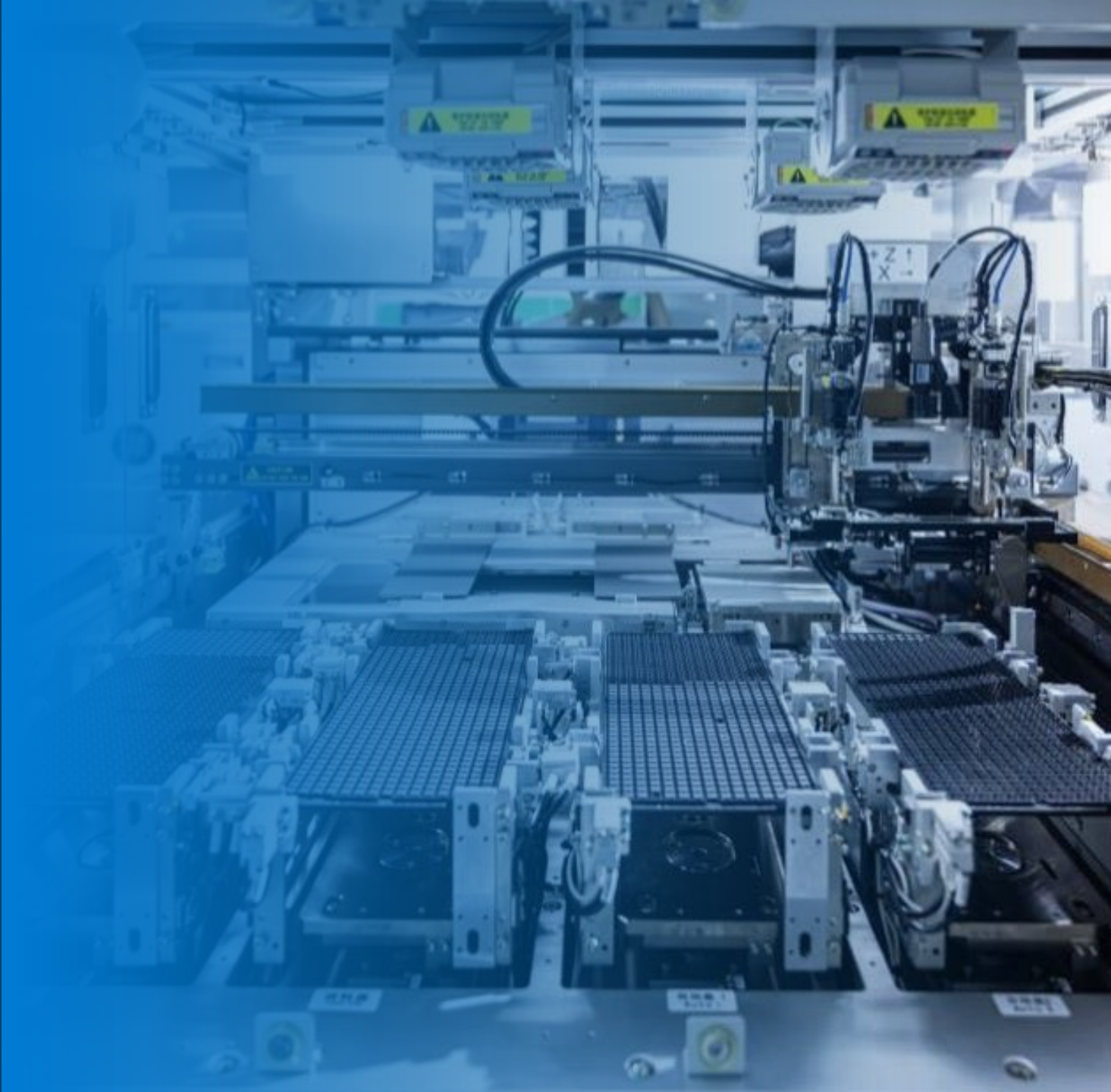


- The slew rate of GaN device can be easily adjusted by external gate resistor.
- As the circuit diagram above, increasing R_{goff} can decrease turn-off speed, and increasing R_{gon} to decrease turn-on speed.
- The R_{gon}/R_{goff} ratio should be well designed, to make sure the false turn-on risk is under control.

PART 04

About us

www.cloudsemi.net



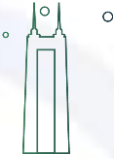
Powering the Dreams



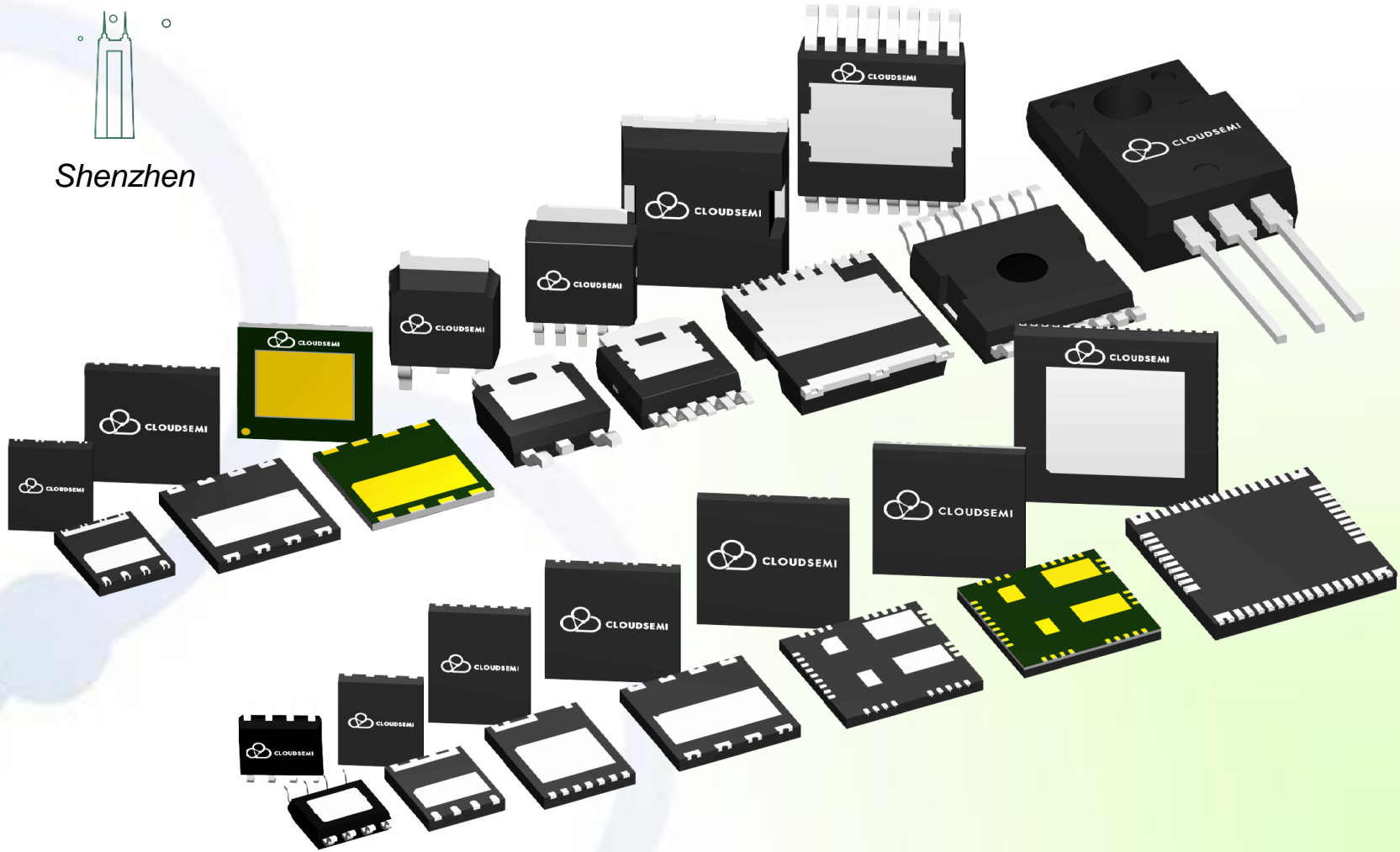
Shanghai



Hangzhou



Shenzhen



Further product information and application support at www.cloudsemi.net

杭州云镓半导体科技有限公司
Hangzhou CloudSemi Technology Co., Ltd

Thanks

Powering the Dreams!



CLOUDSEMI
云镓半导体