High-Performance 650-V GaN Transistor with Integrated Gate Driver

Description

The CGC02102 is a high-performance and highly reliable 650-V enhancement-mode GaN transistor with integrated gate driver, optimized for high-frequency power conversion circuits.

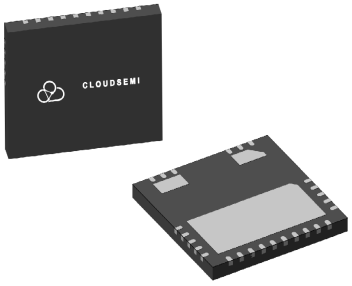
The power GaN transistors in CGC02102, have 650-V drain-source blocking voltage and typical $R_{DS(ON)}$ of 50 mΩ.

The CGC02102 features wide logic input range with hysteresis, compatible to traditional Si-based controller. Also, CGC02102 features wide power supply range of 10 ~ 18 V. The gate drive voltage VDD of 6V is stably provided by internal LDO, making an easier circuit design.

The integrated under-voltage lock-out (UVLO) protection feature is provided drivers to prevent GaN transistors from operating in low efficiency or dangerous conditions.

The independent SGND and PGND design can make sure a reliable logic input signal and a clean gate driving loop.

The device operates in the industrial temperature ranging from -40°C to 125°C. The device is available in a compact 8 x 8 mm QFN package for a minimized parasitic inductance.



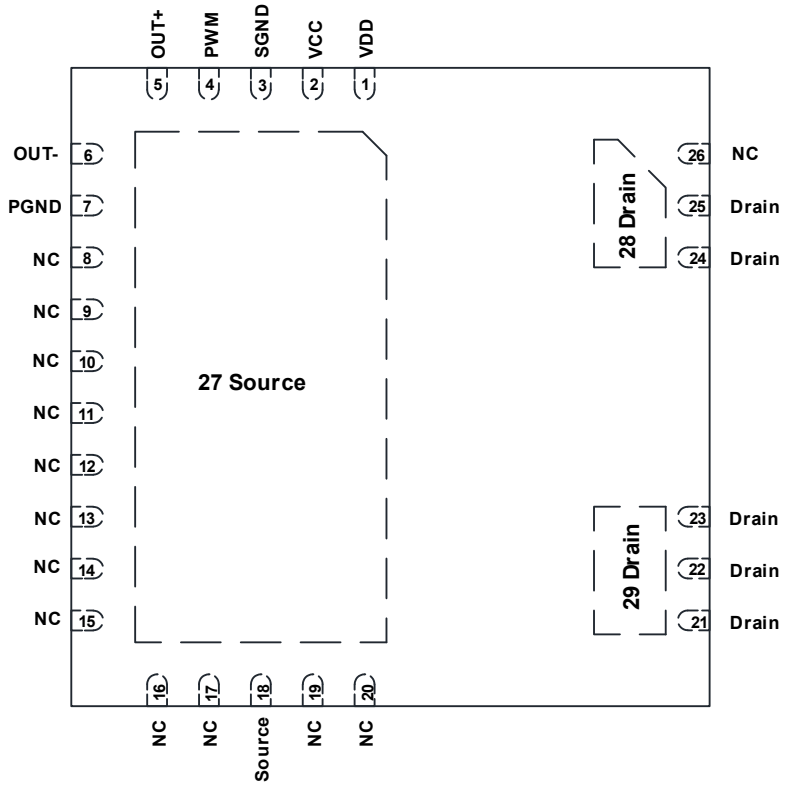
Features

- GaN transistors with integrated gate drive
- 850V transient voltage rating
- 650 V continuous voltage rating
- Zero reverse recovery charge
- Typ./Max. $R_{DS(ON)}$ = 50/65 mΩ
- Wide logic input range with hysteresis
- Wide power supply range (10 V ~ 18 V)
- Internal 6-V LDO for stable gate drive voltage
- Independent SGND and PGND design
- Programmable turn-on dV/dt
- UVLO protection
- ESD protection of 2 kV (HBM), 1 kV (CDM)
- Up to 1 MHz operation
- 8 x 8 mm footprint with large cooling pad
- Minimized package inductance

Typical applications

- AC-DC, DC-DC, DC-AC
- Totem pole PFC, LLC
- Mobile fast-chargers, adapters
- LED lighting, Class-D audio
- Solar micro-inverters
- TV / monitor, wireless power
- Server, telecom & networking SMPS
- Uninterruptable power suppliles (UPS)
- Energy storage systems
- Industrial motor drives

Pin configuration and functions



Package Top View

Pin #	Name	I/O	Description
21~25,28,29	Drain	P	Drain of GaN transistor. MUST connect these drain pads together during PCB design. DON'T split them.
8~17, 19~20, 26	NC	NC	Not connected
1	VDD	I	6V LDO output. This pin provides power to driving stage. Locally bypass this pin to PGND with a ceramic capacitor.
2	VCC	P	Gate driver supply voltage. Locally bypass this pin to SGND with a ceramic capacitor.
3	SGND	G	Logic ground
4	PWM	I	PWM signal logic input
5	OUT+	-	Gate driver turn-on slew-rate set pin (using R_{gon})
6	OUT-	-	Gate driver turn-on slew-rate set pin (using R_{gon})
7	PGND	G	Gate driver ground. Internally connected to Source
18,27	Source	O, G	Source of GaN transistor

I = Input, O = Output, P = Power, G = Ground, NC = No Connect

Ordering information

Ordering Code	Package	Marking	Packing
CGC02102	QFN8*8	CGC02102	Reel

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1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute maximum ratings* may cause permanent damage to the device.

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V, V_{DS} = 850 V
V_{CC}-SGND voltage	V_{CC}	-0.3	-	24	V	
V_{DD}-PGND voltage	V_{DD}	-0.3	-	7	V	
SGND-PGND voltage	V_{SP}	-5	-	5	V	
Continuous current, drain-source	I_D	-	-	30	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	60	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	25	A	T_c = 125 °C
Operating temperature	T_j	-40	-	125	°C	
Storage temperature	T_{stg}	-55	-	150	°C	

Notes

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.

2. Pulse width = 10 μs.

2 Recommended operating conditions

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
V_{CC}-SGND voltage	V_{CC}	10	-	18	V	
PWM input pin voltage	V_{PWM}	0	-	18	V	
Junction temperature	T_j	-40	-	+125	°C	
Ambient temperature	T_a	-40	-	+125	°C	

3 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	–	0.9	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

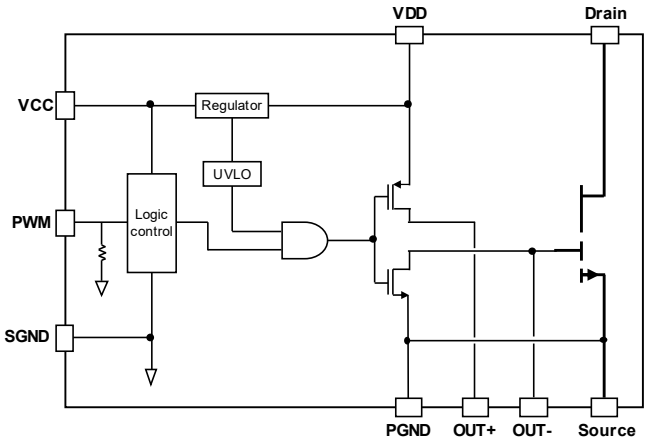
Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{CC} = 12 V

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
V_{CC} Supply Characteristics						
V_{CC} quiescent current	I_{QCC}	-	0.74	-	mA	V_{PWM} = 0 V
V_{CC} operating current	I_{QCC-SW}	-	2	-	mA	F_{SW} = 500 kHz; V_{DS} = open
V_{CC} UVLO rising threshold	V_{CC-ON}	8.1	8.4	8.8	V	
V_{CC} UVLO falling threshold	V_{CC-OFF}	7.5	7.8	8.1	V	
V_{CC} UVLO hysteresis	V_{CC-HYS}	0.4	0.6	-	V	
Low-side logic input Characteristics						
Input pin pull-down resistance	R_{PWM-PD}	-	200	-	kΩ	
Input pin high logic bias current	I_{PWM-H}	-	20	-	μA	
Input logic high threshold (rising edge)	V_{PWMH}	1.7	2.1	2.5	V	
Input logic low threshold (falling edge)	V_{PWML}	0.9	1.2	1.5	V	
Input logic hysteresis	V_{I-HYS}	0.8	0.9	-	V	
Turn-on propagation delay	T_{ON}	-	8.5		ns	V_{DS} = 400 V, I_D = 15 A, L = 90 μH, R_{gon} = 10 Ω
Turn-off propagation delay	T_{OFF}	-	10.7		ns	
Drain rise time	T_R	-	6.4	-	ns	
Drain fall time	T_F	-	5.9	-	ns	
Switching Characteristics						
Switching frequency	F_{SW}	-	-	1	MHz	
Pulse width	T_{PW}	0.02	-	1000	μs	
GaN FET Characteristics						
Drain-source leakage current	I_{DSS}	-	-	55	μA	V_{DS} = 650V; V_{PWM} = 0; T_j = 25°C
		-	100	-		V_{DS} = 650V; V_{PWM} = 0; T_j = 125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	50	65	mΩ	V_{PWM} = 12V; I_D = 9A; T_j = 25 °C
		-	110	-	mΩ	V_{PWM} = 12V; I_D = 9A; T_j = 125 °C
Source-drain reverse voltage	V_{SD}	-	2.9	-	V	V_{PWM} = 0 V; I_{SD} = 15 A
Output charge	Q_{OSS}	-	60	-	nC	V_{PWM} = 0 V; V_{DS} = 0 to 400 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 15 A; V_{DS} = 400 V
Output capacitance	C_{oss}	-	60	-	pF	V_{PWM} = 0 V; V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	102	-	pF	V_{PWM} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	151	-	pF	V_{PWM} = 0 V; V_{DS} = 0 to 400 V

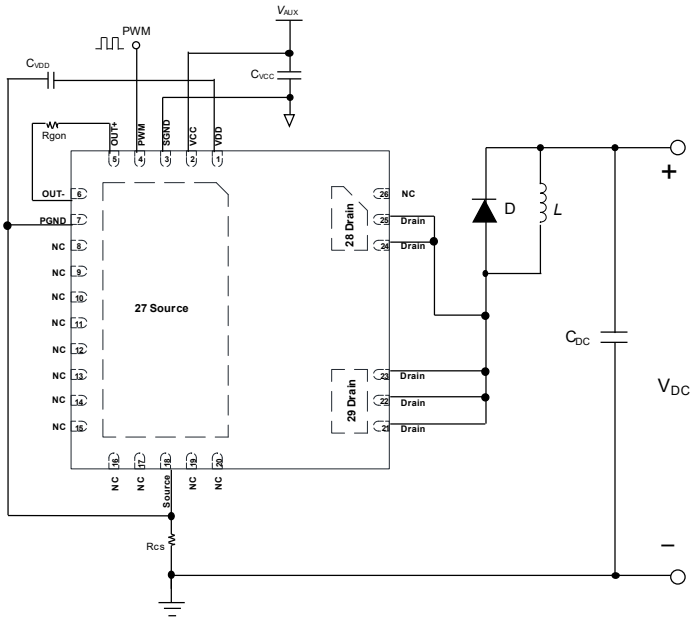
Notes

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

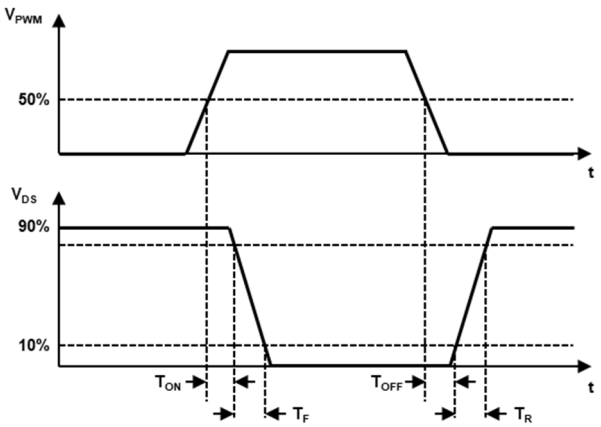
5 Block diagram



6 Switching waveforms



Inductive-load switching circuit

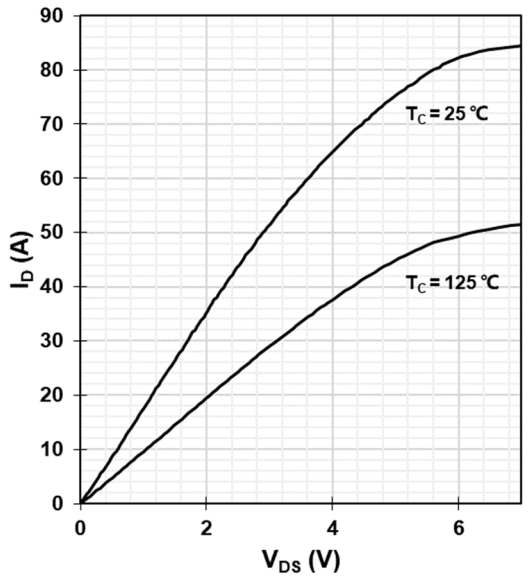


Propagation delay and rise/fall time definitions

7 Electrical characteristics diagrams

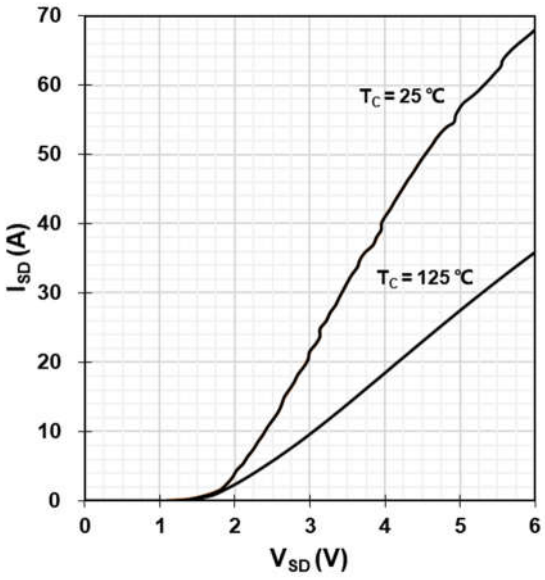
at T_j = 25 °C, unless otherwise noted.

Figure 1 Typ. output characteristics



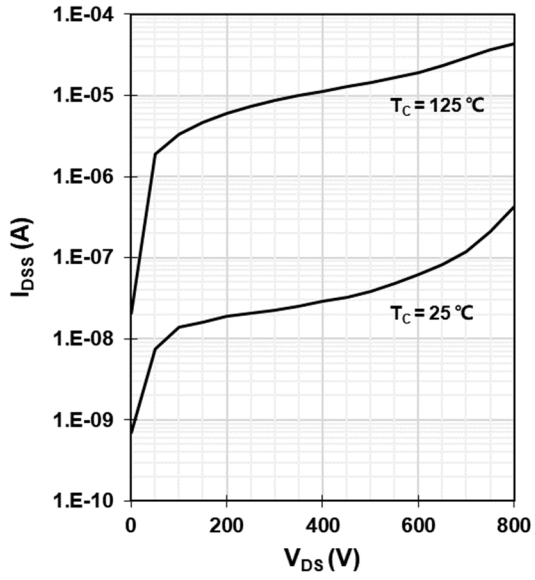
$I_D = f(V_{DS})$; V_{PWM} = 12 V

Figure 2 Typ. channel reverse characteristics



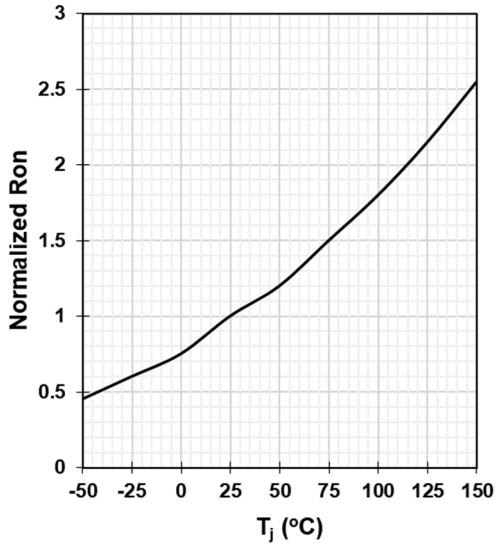
$I_{SD} = f(V_{SD})$; V_{PWM} = 0 V

Figure 3 Typ. drain-source leakage characteristics



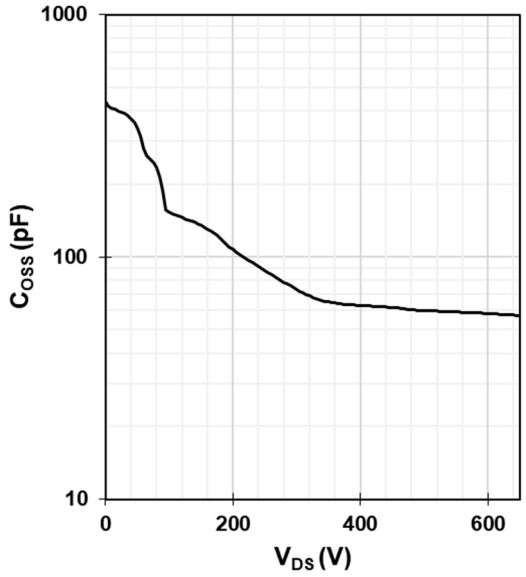
$I_{DSS} = f(V_{DS})$; V_{PWM} = 0 V

Figure 4 Typ. drain-source on-state resistance



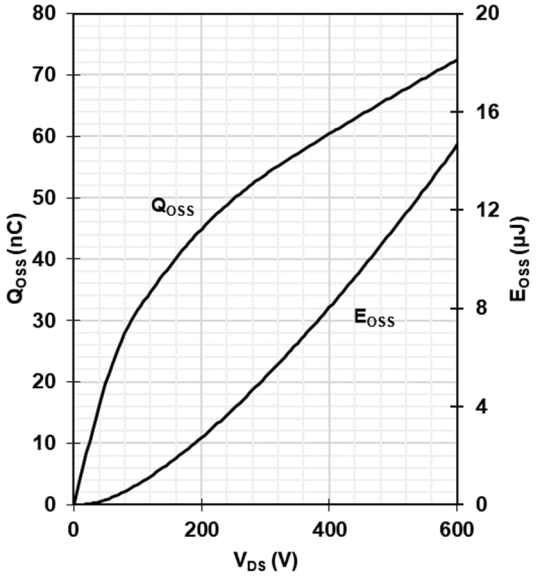
$R_{DS(on)} = f(T_j)$; I_D = 5.3 A; V_{PWM} = 12 V

Figure 5 Typ. output capacitance



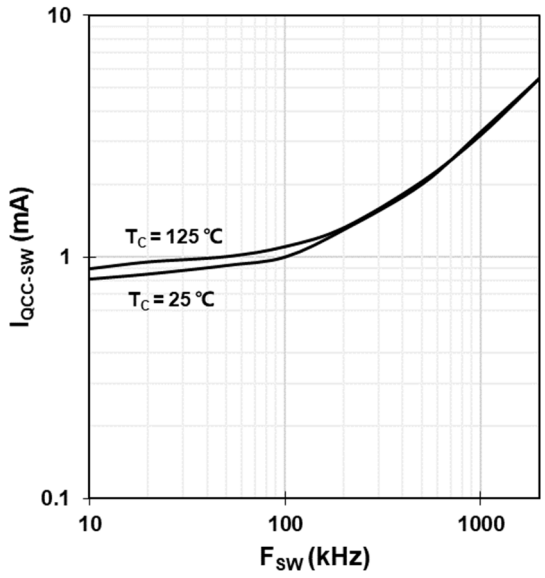
C_{OSS} = f(V_{DS}); Freq. = 1 MHz

Figure 6 Typ. C_{OSS} stored charge & energy



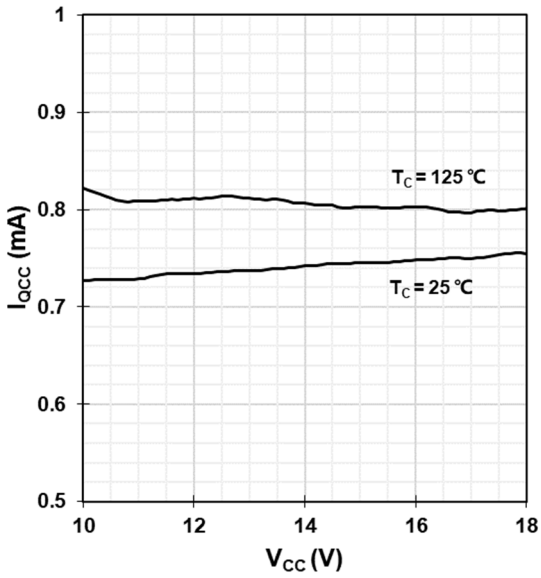
Q_{OSS} = f(V_{DS}); E_{OSS} = f(V_{DS}); Freq. = 1 MHz

Figure 7 VCC operating current (I_{QCC-SW}) vs. F_{SW}

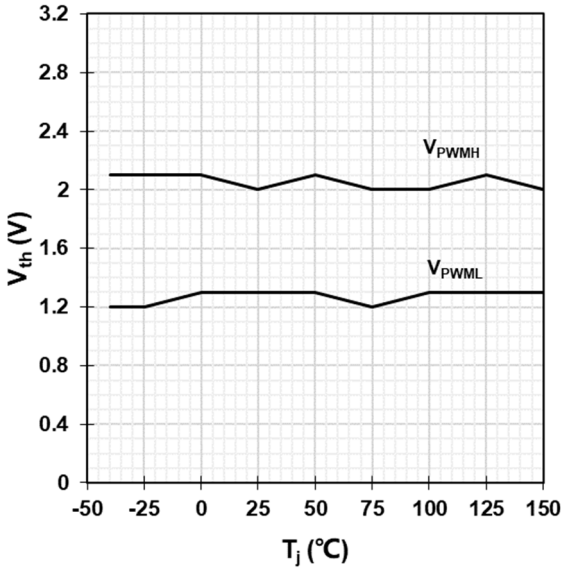
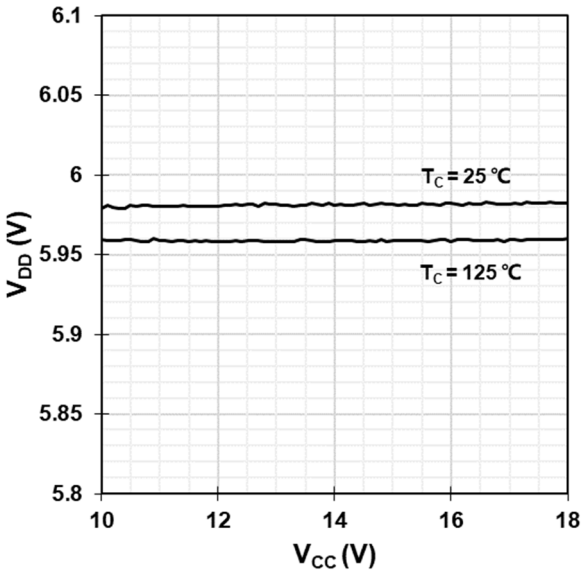


VCC = 12 V, V_{PWM} = 0 V

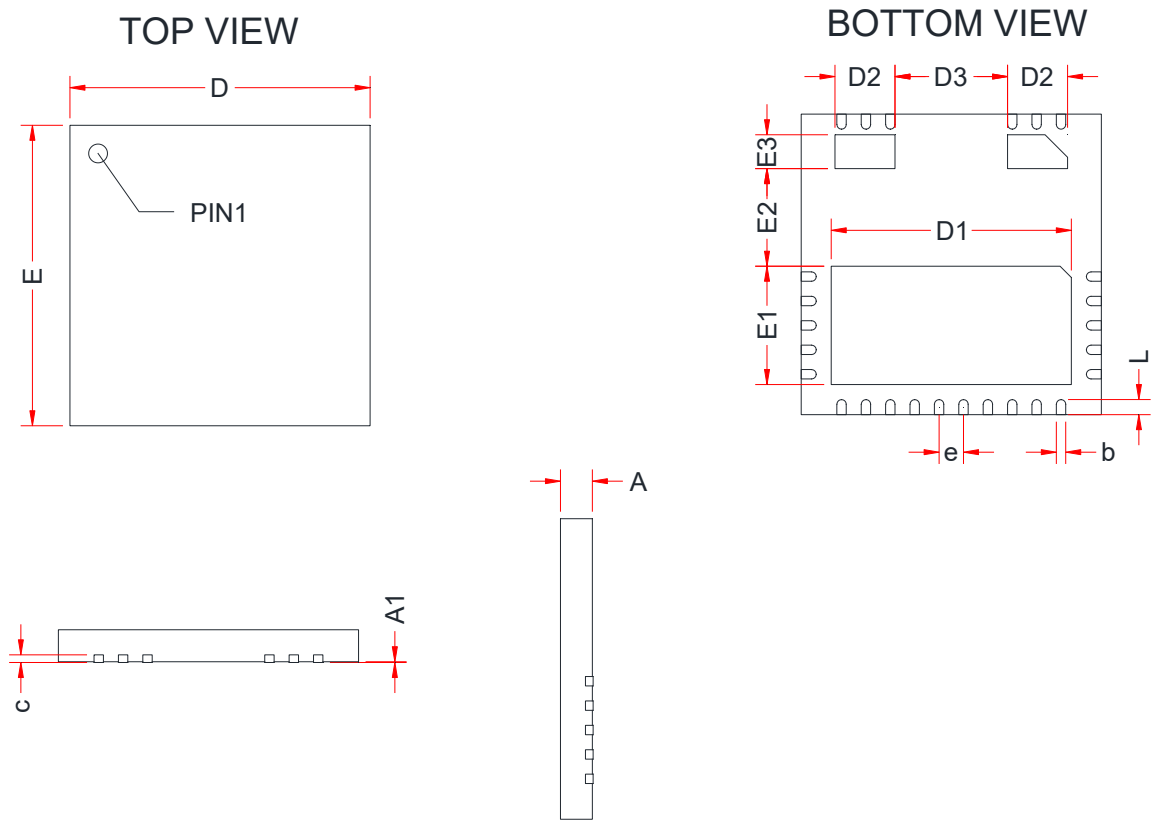
Figure 8 VCC quiescent current (I_{QCC}) vs. V_{CC}

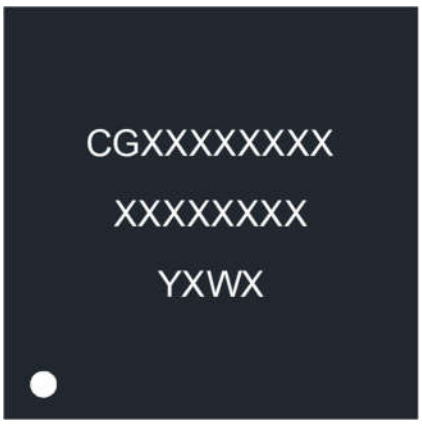


V_{PWM} = 0 V

Figure 9 V_{PWMH} and V_{PWML} vs. T_j	Figure 10 V_{DD} vs. V_{CC}
	
V_{CC} = 12 V	V_{PWM} = 0 V

8 Package outlines

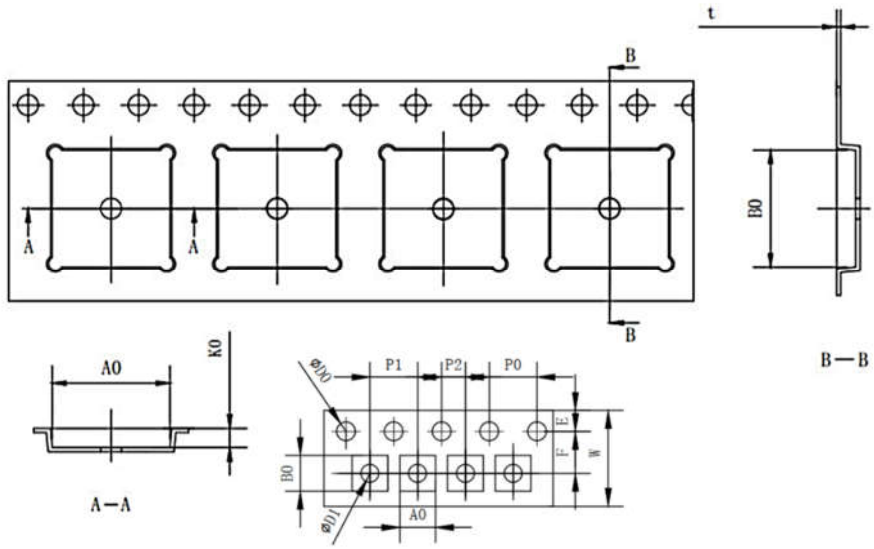




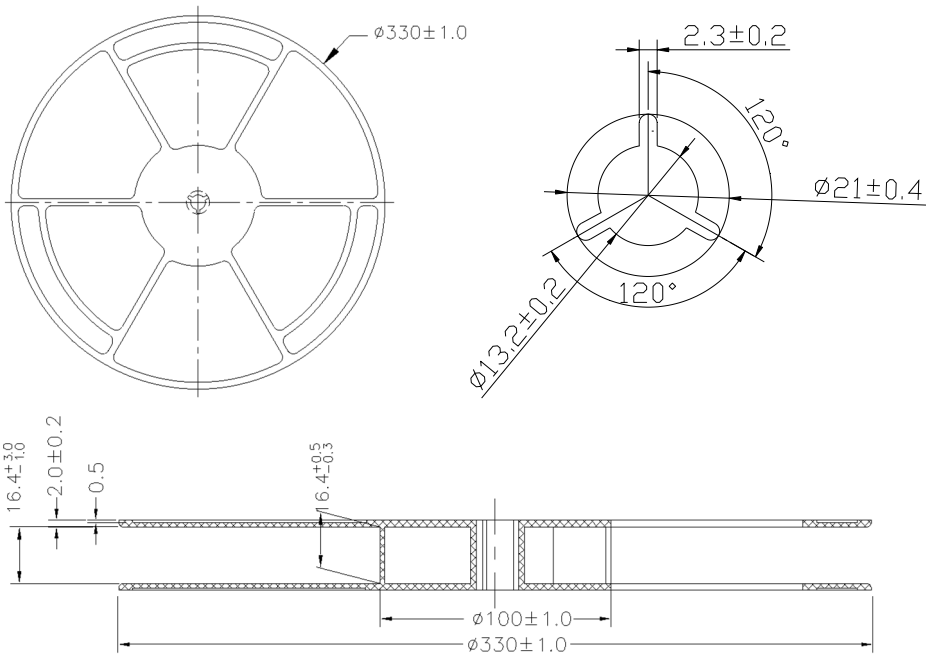
Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	Batch No.	XXXXXXXX
Row 3	Year & Week	YXWX

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	7.90	8.00	8.10
D1	6.30	6.40	6.50
D2	1.50	1.60	1.70
D3	2.90	3.00	3.10
E	7.90	8.00	8.10
E1	3.05	3.15	3.25
E2	2.50	2.60	2.70
E3	0.80	0.90	1.00
e		0.65BSC	
L	0.30	0.40	0.50

9 Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	t	0.30±0.05
P2	2.00±0.10		



10 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-6-1	1.0 version release