CGC02201 Single-Channel Low-Side GaN Gate Driver

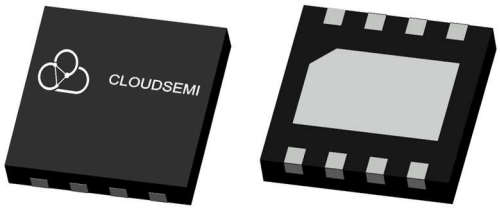
Description

CGC02201 is a single-channel gate driver IC, designed to drive GaN FETs. With strong sink current capability, CGC02201 can drive multiple GaN FETs in parallel. CGC02201 features wide logic input range with hysteresis, compatible to traditional MOSFET controller. Also, CGC02201 features wide power supply range of 10~18 V. The gate drive voltage VDD of 6V is stably provided by internal LDO, making an easier circuit design.

The integrated under-voltage lock-out (UVLO) protection feature is provided drivers to prevent GaN transistors from operating in low efficiency or dangerous conditions.

The independent SGND and PGND design can make sure a reliable logic input signal and a clean gate driving loop.

The driver operates in the temperature ranging from -40°C to +125°C. The device is available in a compact 3 x 3 mm DFN package for a minimized parasitic inductance.



Features

- Single-channel GaN gate driver IC
- Wide logic input range with hysteresis
- Wide power supply range (10 V to 18 V)
- Internal 6-V LDO for stable gate drive voltage
- Independent SGND and PGND design
- Independent source and sink outputs for controllable rise and fall time
- 4-A/2-A peak sink and source drive current
- UVLO protection
- -40°C to +125°C operating temperature range
- 8-PIN DFN3*3 package

Typical applications

- AC/DC, DC/DC, DC/AC
- Totem pole PFC, LLC
- Mobile fast-chargers, adapters
- LED lighting, Class-D audio
- Micro-inverters, energy storage systems
- TV / monitor, wireless power
- Server, telecom & networking SMPS
- Uninterruptable power supplies (UPS)

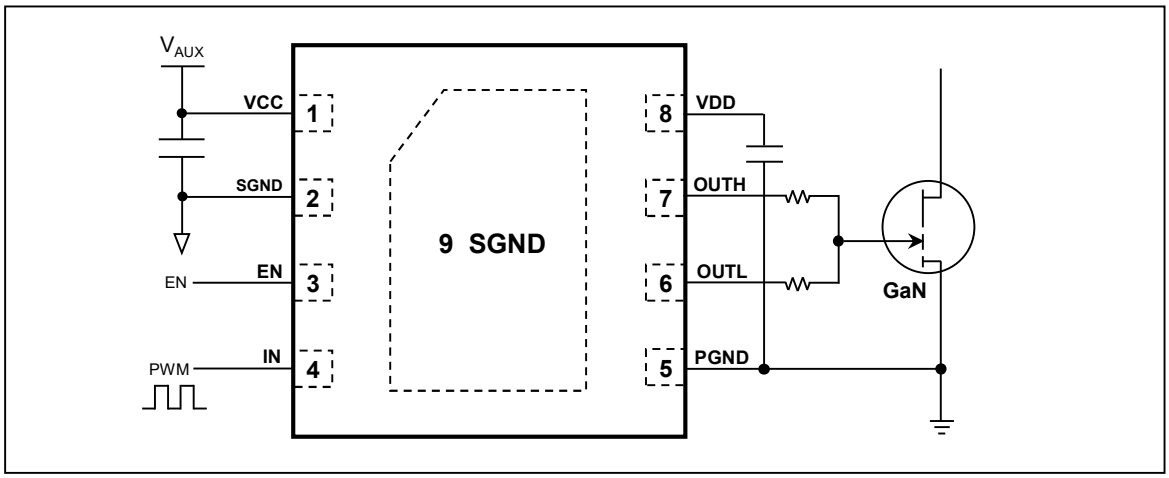


Figure 1 Typical application circuit

Pin configuration and functions

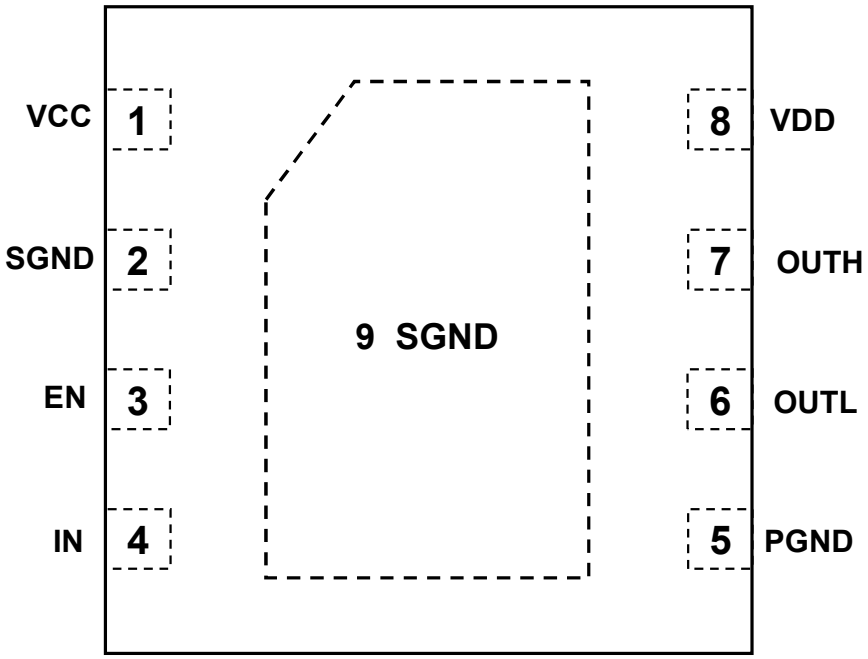


Figure 2 Package 8-PIN DFN3*3 top view

Pin #	Name	I/O	Description
1	V_{CC}	I	Gate driver supply voltage. Locally bypass this pin to SGND with a ceramic capacitor.
2	SGND	G	Logic ground
3	EN	I	Enabling signal logic input
4	IN	I	PWM signal logic input
5	PGND	G	Gate driver ground.
6	OUTL	O	Gate driver turn-off slew-rate set pin
7	OUTH	O	Gate driver turn-on slew-rate set pin
8	V_{DD}	O	6V LDO output. This pin provides power to driving stage. Locally bypass this pin to PGND with a ceramic capacitor.
9	SGND	G	Logic ground.

I = Input, O = Output, G = Ground

Ordering information

Ordering Code	Package	Marking	Packing
CGC02201	8-PIN DFN3*3	CGC02201	Reel

Table of Contents

1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute maximum ratings* may cause permanent damage to the device.

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V_{CC}-SGND voltage	V_{CC}	-0.3	-	24	V	
V_{DD}-PGND voltage	V_{DD}	-0.3	-	7	V	
SGND-PGND voltage	V_{SP}	-5	-	5	V	
Operating temperature	T_j	-40	-	+125	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

2 Recommended operating conditions

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V_{CC}-SGND voltage	V_{CC}	10	-	18	V	
PWM input pin voltage	V_{IN}	0	-	18	V	
Junction temperature	T_j	-40	-	+125	°C	
Ambient temperature	T_a	-40	-	+125	°C	

3 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	0.9	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{CC} = 12 V

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V_{CC} Supply Characteristics						
V_{CC} quiescent current	I_{QCC}	-	0.74	-	mA	V_{IN} = 0 V
V_{CC} operating current	I_{QCC-SW}	-	2	-	mA	F_{SW} = 500 kHz, C_{LOAD} = 100 pF
V_{CC} UVLO rising threshold	V_{CC-ON}	8.1	8.4	8.8	V	
V_{CC} UVLO falling threshold	V_{CC-OFF}	7.5	7.8	8.1	V	
V_{CC} UVLO hysteresis	V_{CC-HYS}	0.4	0.6	-	V	
Logic input Characteristics						
Input pin pull-down resistance	R_{IN-PD}	-	200	-	kΩ	HIN = 3 V
Input pin high logic bias current	I_{IN-H}	-	20	-	μA	HIN = 5 V
Enable pin pull-down resistance	R_{EN_PD}	-	200	-	kΩ	EN = 3 V
Enable pin high logic bias current	I_{EN_H}	-	20	-	μA	EN = 5 V
Input logic high threshold (rising edge)	V_{INH}, V_{ENH}	1.7	2.1	2.5	V	
Input logic low threshold (falling edge)	V_{INL}, V_{ENH}	0.9	1.2	1.5	V	
Input logic hysteresis	V_{IN-HYS}, V_{EN_HYS}	0.8	0.9	-	V	
Driver Output Characteristic						
Regulator Output Voltage	V_{VDD}	5.7	6	6.3	V	C_{VDD} = 100 nF
Driver output pull-down resistance	R_{SNK}	-	1	-	Ω	
Driver output pull-up resistance	R_{SRC}	-	51	-	Ω	
Output peak source current	I_{SRC_PK}	-	2	-	A	
Output peak sink current	I_{SNK_PK}	-	4	-	A	

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
Switching Characteristics						
Switching frequency	F_{SW}	-	-	2	MHz	
Pulse width	T_{PW}	0.02	-	1000	μs	
Turn-on propagation delay	T_{ON}	-	8.5		ns	see Figure 4
Turn-off propagation delay	T_{OFF}	-	10.7		ns	
Output rise time	T_R	-	11	-	ns	C_{LOAD} = 1 nF see Figure 4
Output fall time	T_F	-	5	-	ns	

5 Functional block diagram

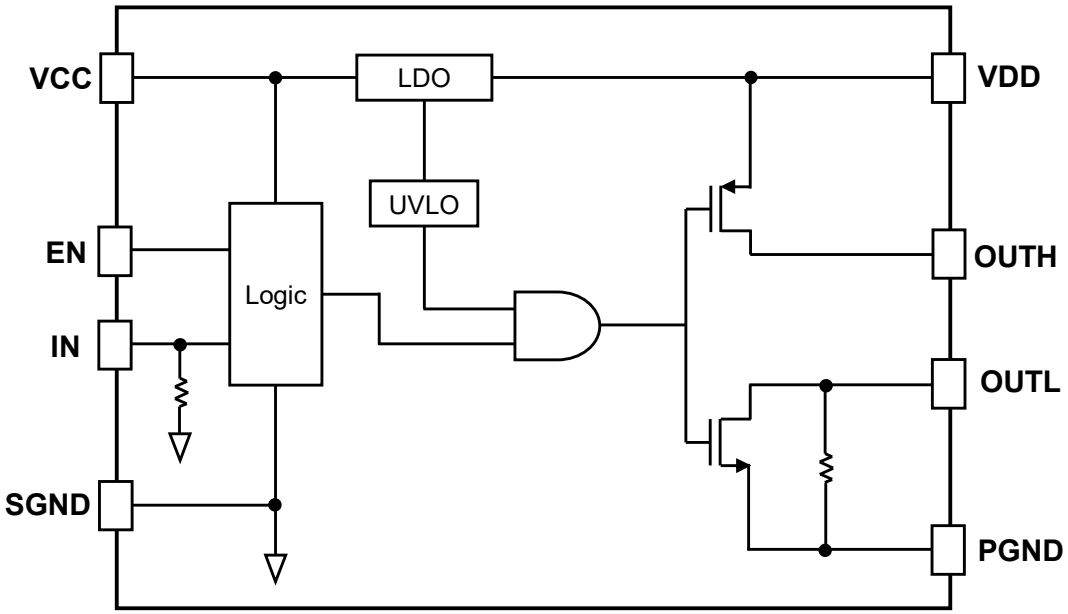


Figure 3 Functional block diagram

6 Timing diagram

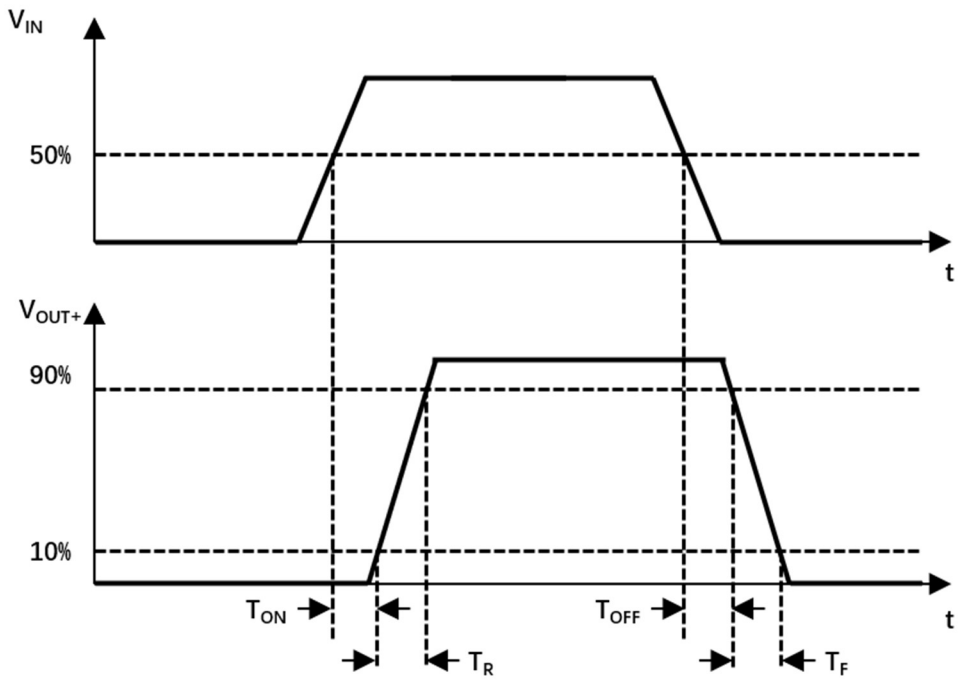
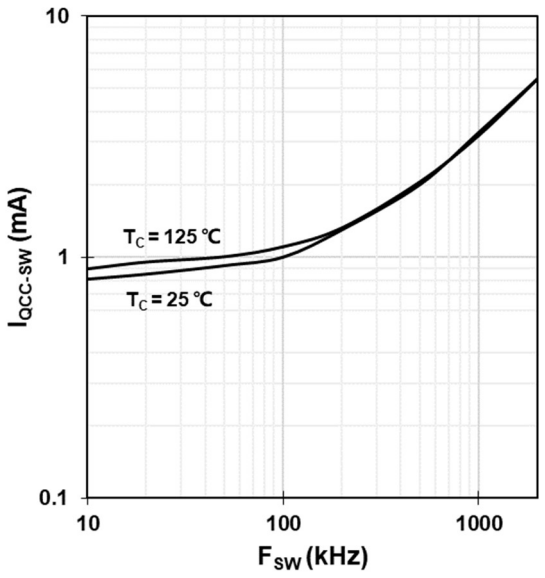


Figure 4 Propagation delay and rise/fall time definitions

7 Electrical characteristics diagrams

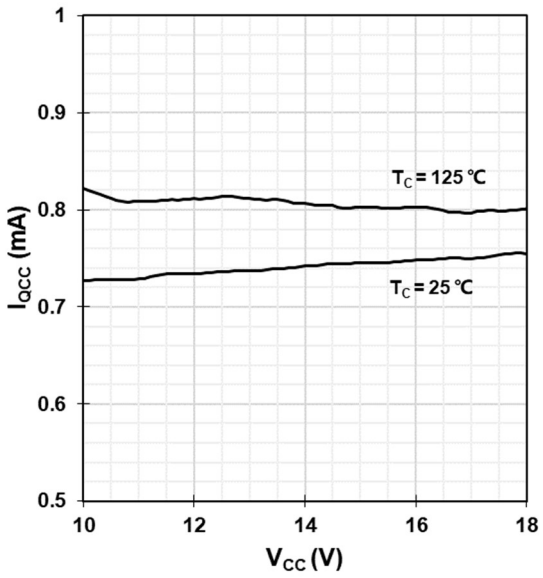
at T_j = 25 °C, unless otherwise specified.

Figure 1 VCC operating current (I_{QCC-SW}) vs. F_{SW}



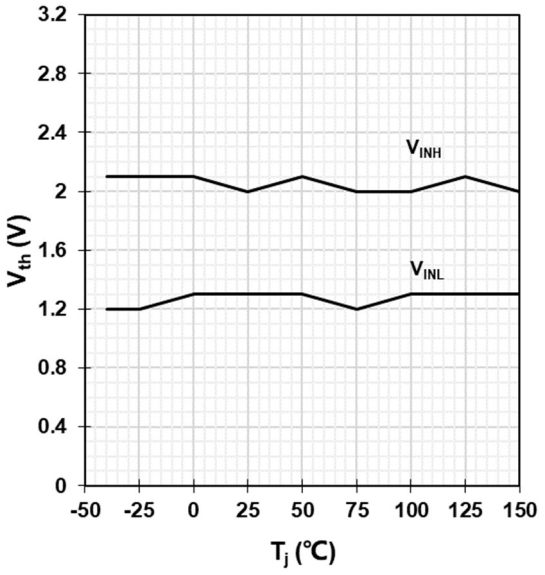
VCC = 12 V, C_{LOAD} = 100 pF

Figure 2 VCC quiescent current (I_{QCC}) vs. V_{CC}



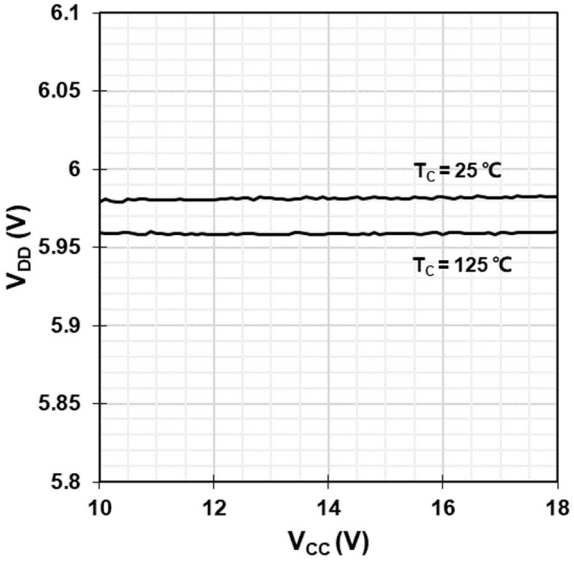
V_{IN} = 0 V

Figure 3 V_{INH} and V_{INL} vs. T_j



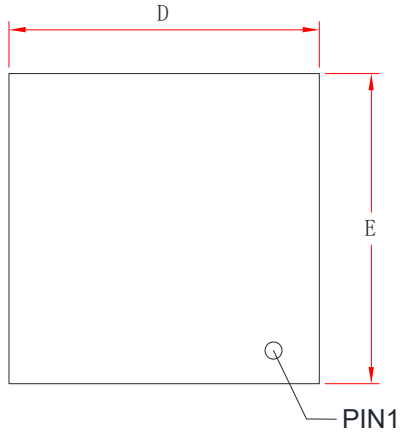
V_{CC} = 12 V

Figure 4 V_{DD} vs. V_{CC}

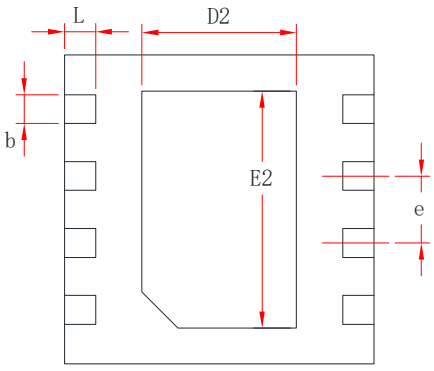


V_{IN} = 0 V

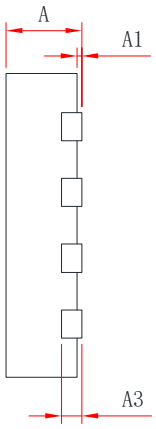
8 Package outlines



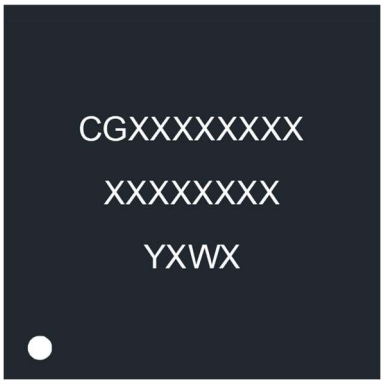
TOP VIEW



BOTTOM VIEW



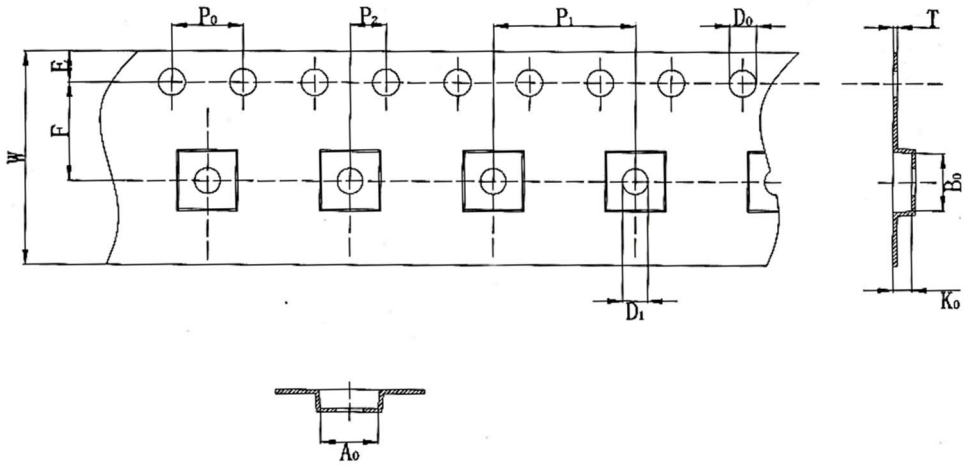
SIDE VIEW



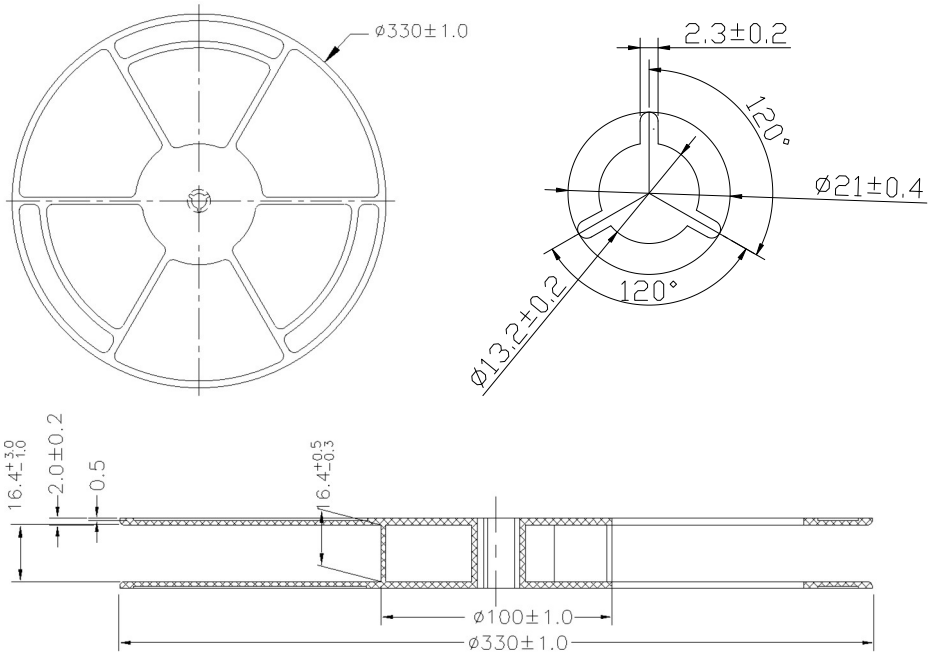
Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	ASSY lot No.	XXXXXXXX
Row 3	Year & Week	YXWX

Symbols	MIN	MID	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
A3		0.203 REF	
b	0.23	0.28	0.33
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	2.20	2.30	2.40
e		0.65 TYP	
L	0.25	0.3	0.35

9 Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	12.00±0.20	10P0	40.00±0.20
E	1.75±0.10	P1	8.00±0.10
F	5.50±0.10	A0	3.23±0.10
D0	1.50±0.10	B0	3.23±0.10
D1	1.50±0.10	K0	1.05±0.10
P0	4.00±0.10	T	0.23±0.05
P2	2.00±0.05		



10 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-5-31	1.0 version release
1.1	2024-7-15	Update pin name and figures