# CG65030TAD

## Description

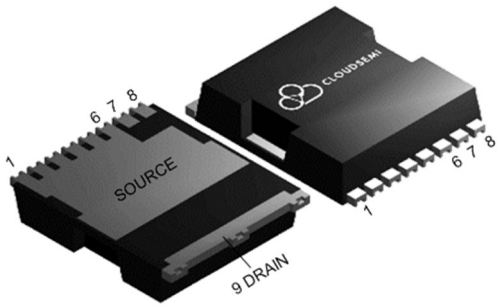
CG65030TAD is a 650V GaN-on-Si enhancement-mode power transistor in TO-Leadless (TOLL) package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The TOLL package offers low parasitic resistance/inductance, strong heat dissipation and high solderability, which can fully release device potential and make GaN better apply to industrial applications.

## Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- On board charger (OBC)
- Charging pile
- Traction inverter
- Industrial motor drives

## Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on),\ max}$ 30mΩ
- Recommended gate drive voltage 0V ~ 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3
- RoHS, Pb-free, REACH-compliant



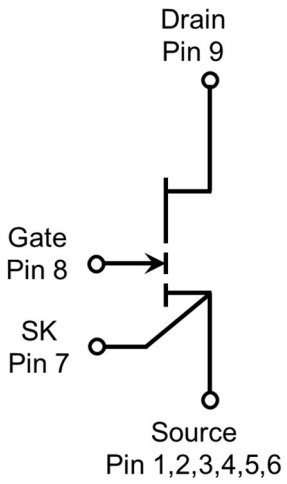




**Table 1 Key Performance Parameters at $T_j$ = 25 °C**

| Parameters | Values | Units |
|---|---|---|
| $V_{DS,\ max}$ | 650 | V |
| $R_{DS(on),\ max}$ | 30 | mΩ |
| $Q_{G,\ typ}$ | 14.3 | nC |
| $I_{D,\ Pulse}$ | 120 | A |
| $Q_{OSS}$ @ 400 V | 133 | nC |
| $Q_{rr}$ | 0 | nC |

**Table 2 Ordering Information**

| Ordering Code | Package | Marking | Packing |
|---|---|---|---|
| CG65030TAD | TOLL | CG65030TAD | Reel |

# Table of Contents

# 1 Maximum ratings

at $T_j$ = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

**Table 3 Maximum ratings**

| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source voltage | $V_{DS, max}$ | - | - | 650 | V | $V_{GS}$ = 0 V; $I_D$ = 10 μA |
| Drain-source voltage transient [1] | $V_{DS, transient}$ | - | - | 850 | V | $V_{GS}$ = 0 V; $V_{DS}$ = 850 V |
| Continuous current, drain-source | $I_D$ | - | - | 60 | A | $T_c$ = 25 °C |
| Pulsed current, drain-source [2] | $I_{D, pulse}$ | - | - | 120 | A | $T_c$ = 25 °C; $V_G$ = 6 V |
| Pulsed current, drain-source [2] | $I_{D, pulse}$ | - | - | 50 | A | $T_c$ = 150 °C; $V_G$ = 6 V |
| Gate-source voltage, continuous [3] | $V_{GS}$ | -7 | - | +7 | V | $T_j$ = -55 °C to 150 °C |
| Gate-source voltage, pulsed | $V_{GS, pulse}$ | -20 | - | +10 | V | $T_j$ = -55 °C to 150 °C; $t_{Pulse}$ = 50 ns; f = 100 kHz; open drain |
| Power dissipation | $P_{tot}$ | - | - | 278 | W | $T_c$ = 25 °C |
| Operating temperature | $T_j$ | -55 | - | +150 | °C | |
| Storage temperature | $T_{stg}$ | -55 | - | +150 | °C | |

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, $t_{Pulse}$ < 1 μs.
2. Pulse width = 10 μs.
3. The minimum $V_{GS}$ is clamped by ESD protection circuit, as shown in Figure 8.

# 2 Thermal characteristics

**Table 4 Thermal characteristics**

| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction-case | $R_{thJC}$ | - | - | 0.45 | °C/W | |
| Thermal resistance, junction-ambient [1] | $R_{thJA}$ | - | - | 28 | °C/W | |
| Reflow soldering temperature | $T_{sold}$ | - | - | 260 | °C | MSL3 |

1. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12mil) with 0.889 mm pitch (35mil). The copper layers under the thermal pad and drain pad are 25 x 25 $mm^2$ each. The PCB is mounted in horizontal position without air stream cooling.

# 3 Electrical characteristics

at $T_j$ = 25 °C, unless otherwise specified.

**Table 5 Static characteristics**

| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate threshold voltage | $V_{GS(TH)}$ | 1.1 | 1.7 | 2.6 | V | $I_D$ = 15 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C |
| | | - | 1.9 | - | | $I_D$ = 15 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C |
| Drain-source leakage current | $I_{DSS}$ | - | 2 | 50 | μA | $V_{DS}$ = 650 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C |
| | | - | 35 | - | | $V_{DS}$ = 650 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 150 | - | μA | $V_{GS}$ = 6 V; $V_{DS}$ = 0 V |
| Reverse Gate leakage current | $I_{RGL}$ | - | -15 | - | nA | $V_{GS}$ = -6 V; $V_{DS}$ = 0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 25 | 30 | mΩ | $V_{GS}$ = 6 V; $I_D$ = 20 A; $T_j$ = 25 °C |
| | | - | 55 | - | mΩ | $V_{GS}$ = 6 V; $I_D$ = 20 A; $T_j$ = 150 °C |
| Gate resistance | $R_G$ | - | 1.0 | - | Ω | f = 5 MHz; open drain |

**Table 6 Dynamic characteristics**

| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 500 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 1 MHz |
| Output capacitance | $C_{oss}$ | - | 129 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 1 MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 0.94 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 1 MHz |
| Effective output capacitance, energy related [1] | $C_{o(er)}$ | - | 228 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 0 to 400 V |
| Effective output capacitance, time related [2] | $C_{o(tr)}$ | - | 334 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 0 to 400 V |
| Output charge | $Q_{OSS}$ | - | 133 | - | nC | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 1 MHz |
| Output Capacitance Stored Energy | $E_{OSS}$ | - | 18 | - | μJ | |
| Turn-on delay time | $t_{d(on)}$ | - | 4.5 | - | ns | $V_{DS}$ = 400 V; $I_D$ = 20 A; L = 120 μH; $V_{GS}$ = 6 V; $R_{on}$ = 10 Ω; $R_{off}$ = 1 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 13.8 | - | ns | |
| Rise time | $t_r$ | - | 11.5 | - | ns | |
| Fall time | $t_f$ | - | 19.2 | - | ns | |
| Switching Energy during turn-on | $E_{on}$ | - | 136 | - | μJ | |
| Switching Energy during turn-off | $E_{off}$ | - | 18 | - | μJ | |

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V.

**Table 7 Gate charge characteristics**

| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate charge | $Q_G$ | - | 14.3 | - | nC | $V_{GS}$ = 0 to 6 V; $V_{DS}$ = 400 V; $I_D$ = 60 A |
| Gate-source charge | $Q_{GS}$ | - | 3.7 | - | nC | |
| Gate-drain charge | $Q_{GD}$ | - | 3.7 | - | nC | |
| Gate plateau voltage | $V_{plat}$ | - | 2.8 | - | V | $V_{DS}$ = 400 V; $I_D$ = 60 A |

**Table 8 Reverse conduction characteristics**

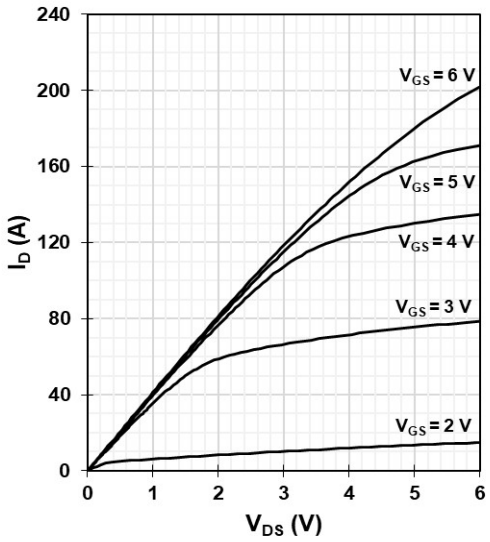
| Parameters | Sym. | Values | | | Units | Notes/Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Source-drain reverse voltage | $V_{SD}$ | - | 3.8 | - | V | $V_{GS}$ = 0 V; $I_{SD}$ = 60 A |
| Pulsed current, reverse | $I_{S,\ pulse}$ | - | 80 | - | A | $V_{GS}$ = 6 V |
| Reverse recovery charge [1] | $Q_{rr}$ | - | 0 | - | nC | $I_{SD}$ = 60 A; $V_{DS}$ = 400 V |
| Reverse recovery time | $t_{rr}$ | - | 0 | - | ns | |
| Peak reverse recovery current | $I_{rrm}$ | - | 0 | - | A | |

1. Excluding $Q_{OSS}$

# 4 Electrical characteristics diagrams

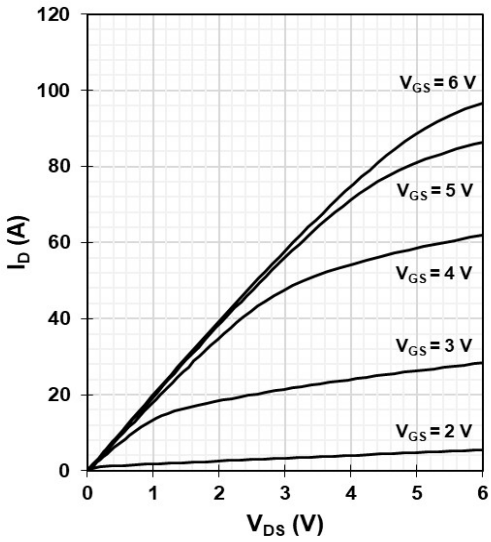
at $T_j$ = 25 °C, unless otherwise specified.

**Figure 1 Typ. output characteristics**



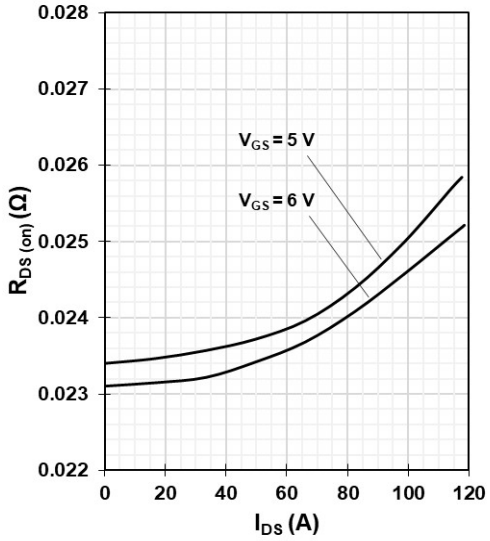

$I_D = f(V_{DS}, V_{GS})$; $T_j$ = 25 °C

**Figure 2 Typ. output characteristics**



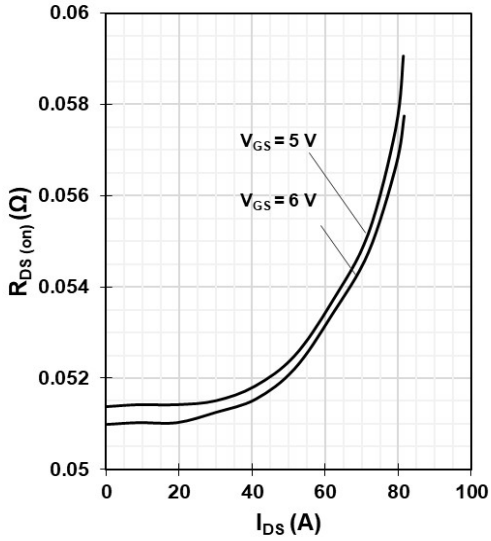

$I_D = f(V_{DS}, V_{GS})$; $T_j$ = 150 °C

**Figure 3 Typ. drain-source on-state resistance**

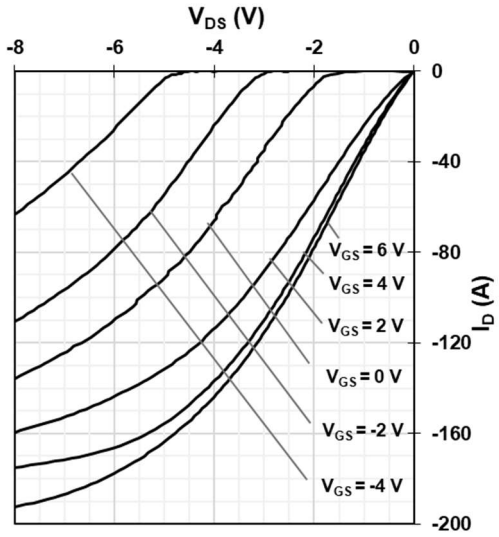
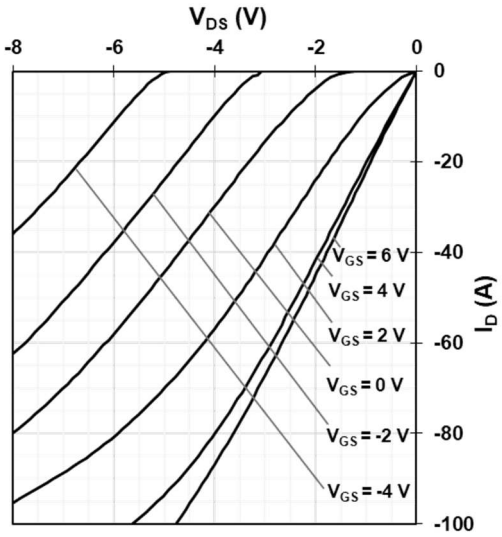



$R_{DS(on)} = f(I_{DS}, V_{GS})$; $T_j$ = 25 °C

**Figure 4 Typ. drain-source on-state resistance**

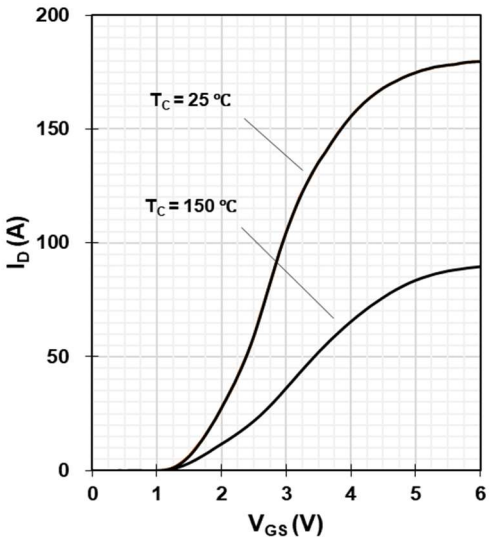
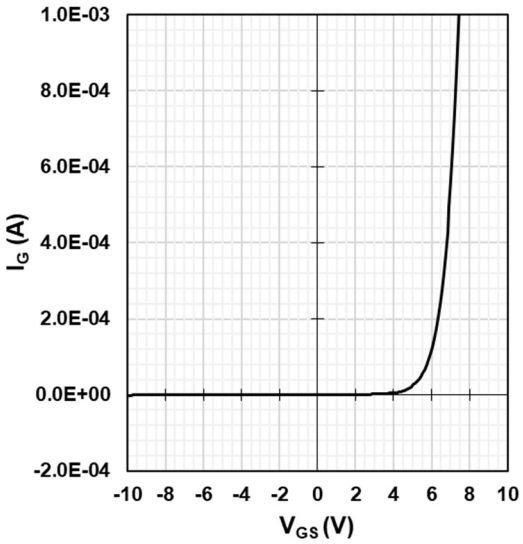


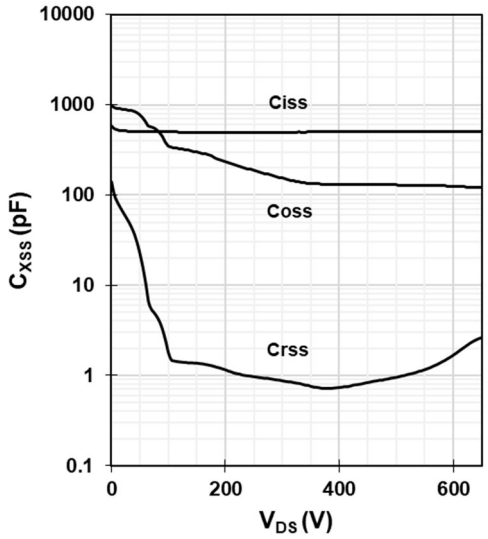
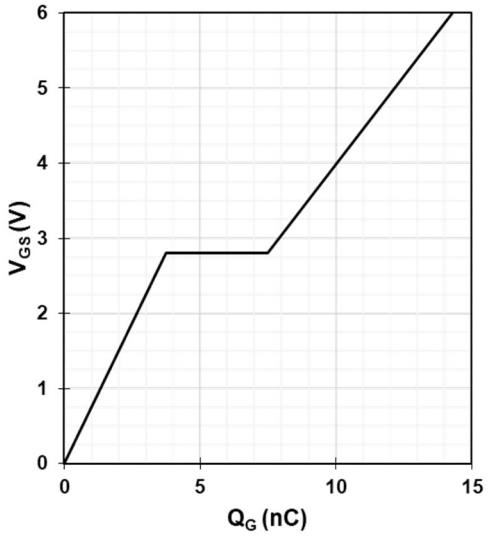

$R_{DS(on)} = f(I_{DS}, V_{GS})$; $T_j$ = 150 °C

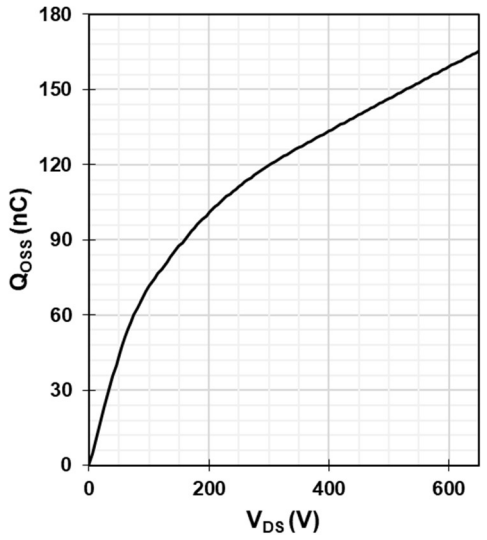
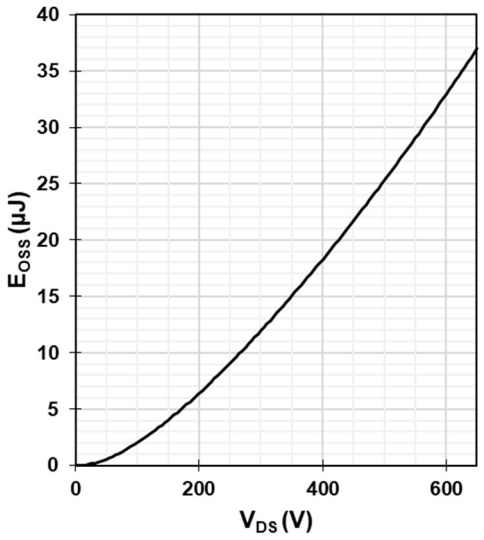
| Figure 5 Typ. channel reverse characteristics | Figure 6 Typ. channel reverse characteristics |
|---|---|
|  |  |
| $I_D = f(V_{DS}, V_{GS})$; $T_j$ = 25 ºC | $I_D = f(V_{DS}, V_{GS})$; $T_j$ = 150 ºC |

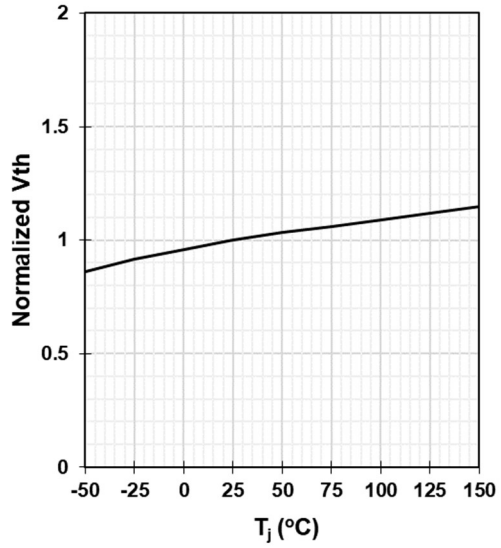
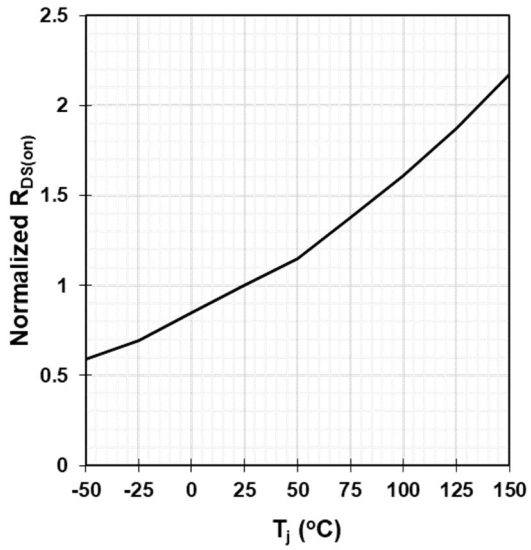




| Figure 7 Typ. transfer characteristics | Figure 8 Typ. gate-to-source leakage |
|---|---|
|  |  |
| $I_D = f(V_{GS})$; $V_{DS}$ = 5 V | $I_G = f(V_{GS})$; $V_D$ = open |

| Figure 9 Typ. capacitances | Figure 10 Typ. gate charge |
|---|---|
|  |  |
| $C_{XSS}$ = f($V_{DS}$); Freq. = 1 MHz | $V_{GS}$ = f($Q_G$); $V_{DS}$ = 400 V; $I_D$ = 60 A |

| Figure 11 Typ. output charge | Figure 12 Typ. $C_{oss}$ stored energy |
|---|---|
|  |  |
| $Q_{OSS}$ = f($V_{DS}$); Freq. = 1 MHz | $E_{OSS}$ = f($V_{DS}$); Freq. = 1 MHz |

| Figure 13 Gate threshold voltage | Figure 14 Drain-source on-state resistance |
|---|---|
|  |  |
| $V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D$ = 15 mA | $R_{DS(on)} = f(T_j)$; $I_D$ = 20 A; $V_{GS}$ = 6 V |

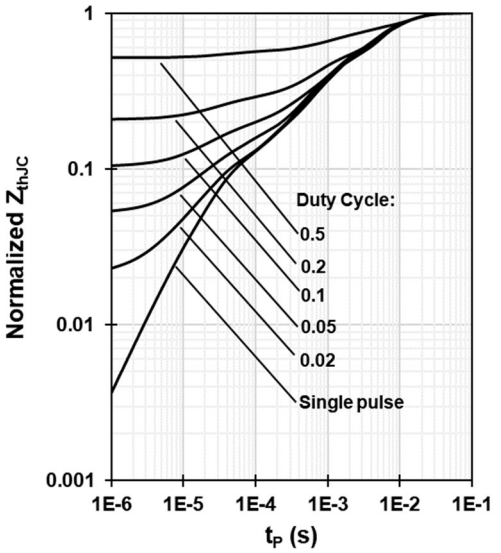
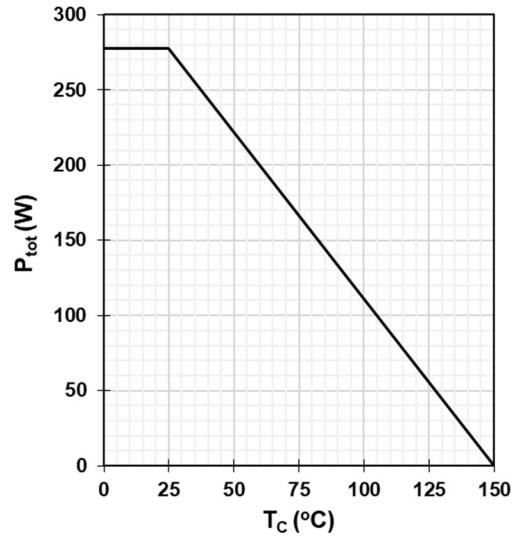
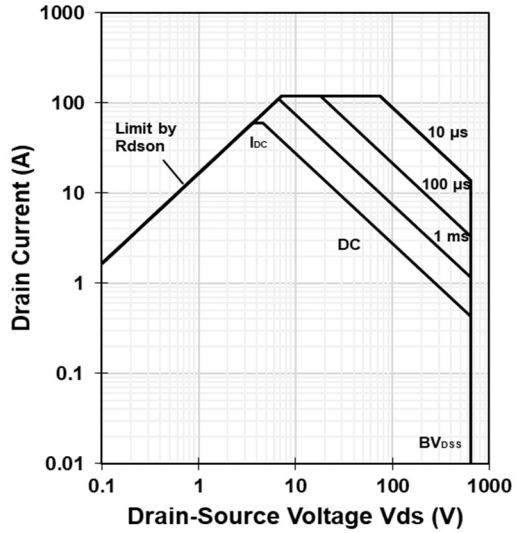
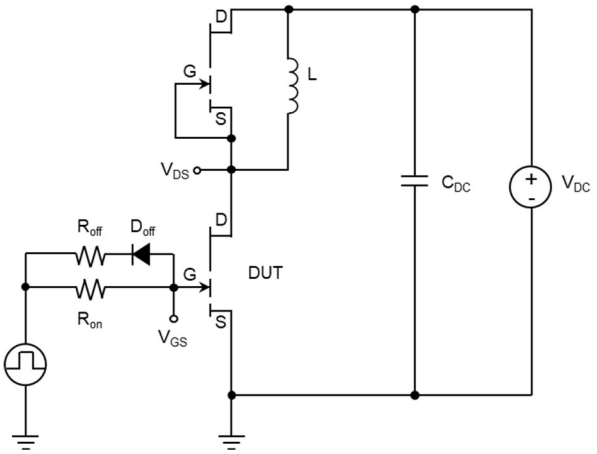
| Figure 15 Max. transient thermal impedance | Figure 16 Power dissipation |
|---|---|
|  |  |
| $Z_{thJC} = f(t_P, D)$ | $P_{tot} = f(T_C)$ |

**Figure 17 Safe operating area**



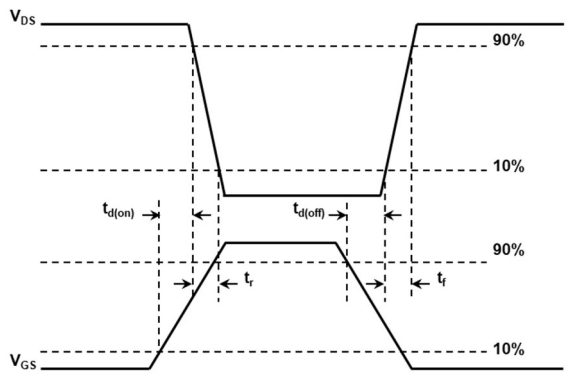

$I_D = f(V_{DS})$; $T_C$ = 25 °C

**Figure 18 Switching time test circuit**

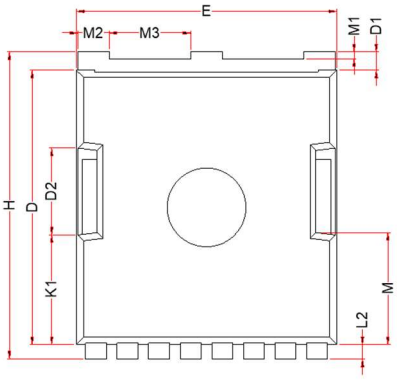


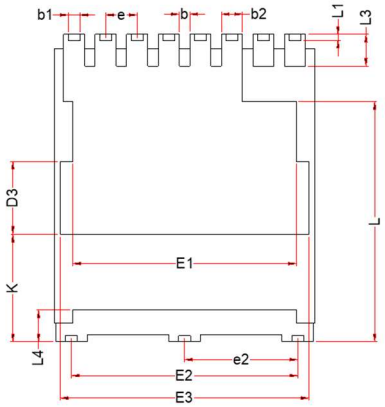

$V_{DS}$ = 400 V, $I_D$ = 20 A, L = 120 µH, $V_{GS}$ = 6 V,
$R_{on}$ = 10 Ω, $R_{off}$ = 1 Ω

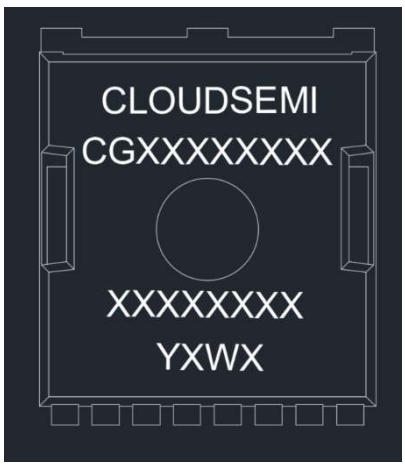
**Figure 19 Typ. switching time waveform**



# 5 Package outlines



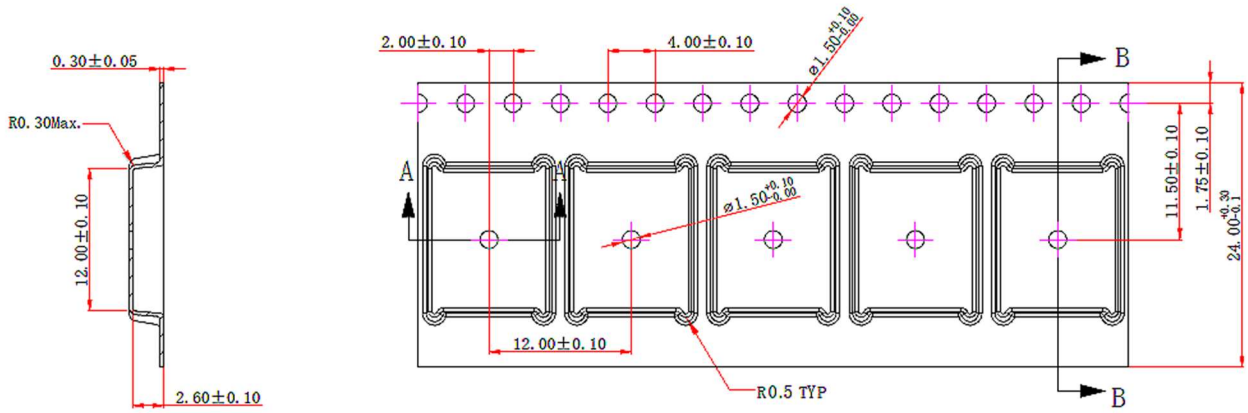



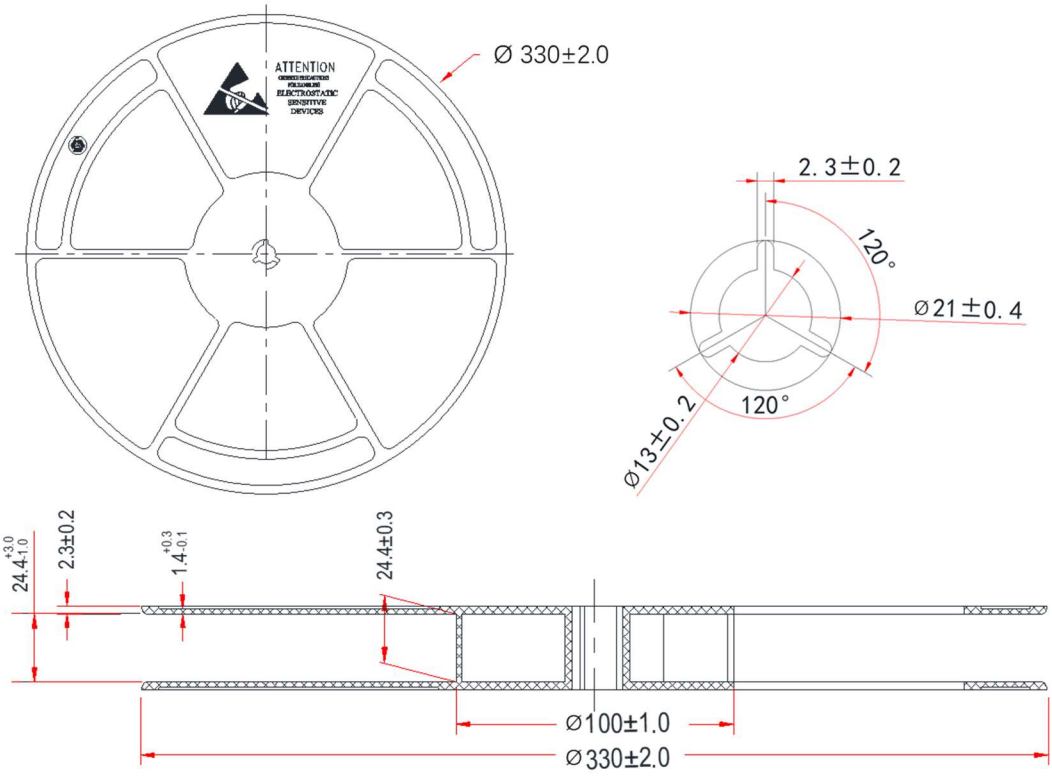




| Row | Description | Example |
|---|---|---|
| Row 1 | Company Logo | CLOUDSEMI |
| Row 2 | Device name | CGXXXXXXXX |
| Row 3 | ASSY lot No. | XXXXXXXX |
| Row 4 | Year & Week | YXWX |

| SYMBOL | MIN | MAX |
|---|---|---|
| A | 2.20 | 2.40 |
| b | 0.30 | 0.50 |
| b1 | 0.35 | 0.55 |
| b2 | 0.70 | 0.90 |
| c | 0.40 | 0.60 |
| D | 10.28 | 10.58 |
| D1 | 0.60 | 0.80 |
| D2 | (3.30) | |
| D3 | (2.77) | |
| E | 9.70 | 10.10 |
| E1 | (8.50) | |
| E2 | (8.50) | |
| E3 | (9.46) | |
| e | 1.10 | 1.30 |
| H | 11.48 | 11.88 |
| K | (4.08) | |
| K1 | (4.17) | |
| L | (9.13) | |
| L1 | 0.13 | 0.33 |
| L2 | 0.50 | 0.70 |
| L3 | 1.10 | 1.30 |
| L4 | 1.10 | 1.30 |
| M | (4.23) | |
| M1 | 0.16 | 0.36 |
| M2 | 1.10 | 1.30 |
| M3 | 3.00 | 3.20 |
| θ | 4° | 10° |
| e2 | 4.20 | 4.40 |

# 6 Tape and reel information



# 7 Revision history

Major changes since the last revision.

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 2024-04-16 | 1.0 version release |
| 1.1 | 2024-08-07 | Laser marking revision |
| 1.2 | 2024-11-18 | Update reverse gate leakage current |