CG65080TAA

Description

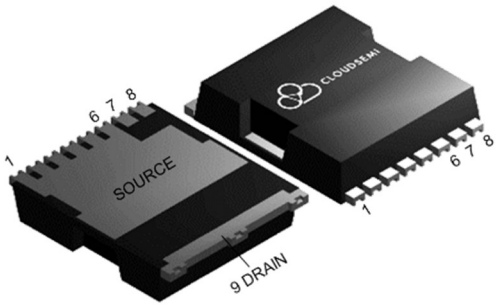
CG65080TAA is a 650V GaN-on-Si enhancement-mode power transistor in TO-Leadless (TOLL) package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The TOLL package offers low parasitic resistance/inductance, strong heat dissipation and high solderability, which can fully release device potential and make GaN better apply to industrial applications.

Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on),\ max}$ 80mΩ
- Recommended gate drive voltage 0V ~ 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3
- RoHS, Pb-free, REACH-compliant

Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- On board charger (OBC)
- Charging pile
- Traction inverter
- Industrial motor drives



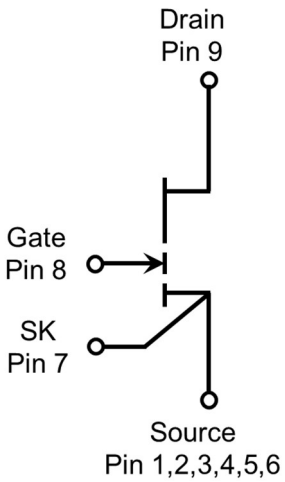


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	650	V
$R_{DS(on),\ max}$	80	mΩ
$Q_{G,\ typ}$	6	nC
$I_{D,\ Pulse}$	42	A
Q_{OSS} @ 400 V	60	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Ordering Code	Package	Marking	Packing
CG65080TAA	TOLL	CG65080TAA	Reel

Table of Contents

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum rating

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V, V_{DS} = 850 V
Continuous current, drain-source	I_D	-	-	22	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	42	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	23	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous [3]	V_{GS}	-7	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	278	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Pulse width = 10 μs.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	0.45	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.7	2.5	V	I_D = 30 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 30 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	5	65	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	100	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	163	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	70	80	mΩ	V_{GS} = 6 V; I_D = 8 A; T_j = 25 °C
		-	135	-	mΩ	V_{GS} = 6 V; I_D = 8 A; T_j = 125 °C
Gate resistance	R_G	-	1.5	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	230	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	71	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.13	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	98	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	152	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	60	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	3.8	-	ns	V_{DS} = 400 V; I_D = 6 A; L = 120 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 1 Ω
Turn-off delay time	$t_{d(off)}$	-	7.5	-	ns	
Rise time	t_r	-	5.0	-	ns	
Fall time	t_f	-	10.2	-	ns	
Switching Energy during turn-on	E_{on}	-	45	-	μJ	
Switching Energy during turn-off	E_{off}	-	8	-	μJ	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	6	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 8 A
Gate-source charge	Q_{GS}	-	0.5	-	nC	
Gate-drain charge	Q_{GD}	-	2	-	nC	
Gate plateau voltage	V_{Plat}	-	2.2	-	V	V_{DS} = 400 V; I_D = 8 A

Table 8 Reverse conduction characteristics

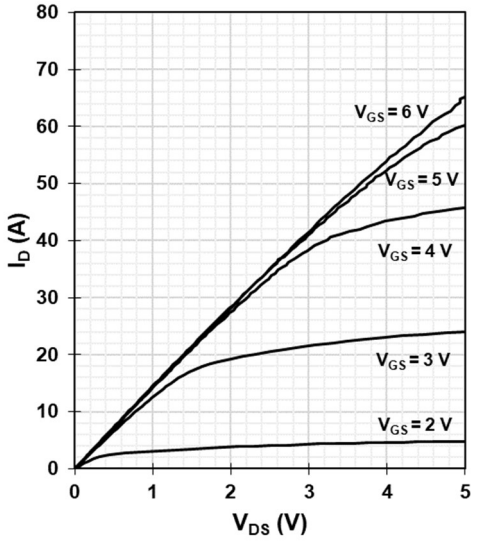
Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.3	-	V	V_{GS} = 0 V; I_{SD} = 8 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	42	-	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 8 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

4 Electrical characteristics diagrams

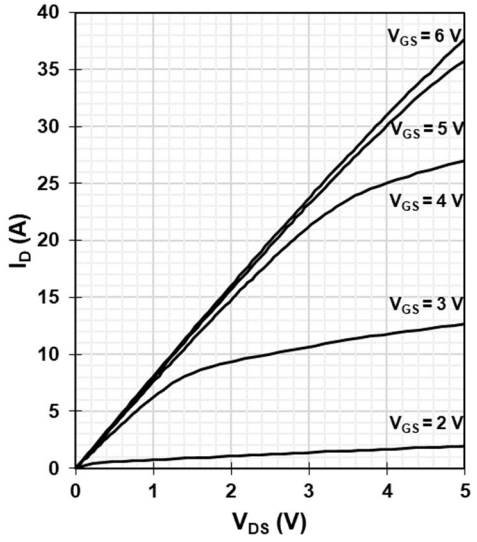
at T_j = 25 ºC, unless specified otherwise.

Figure 1 Typ. output characteristics



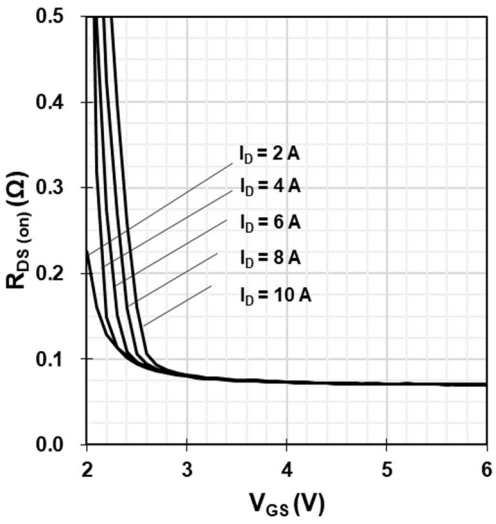
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 ºC

Figure 2 Typ. output characteristics



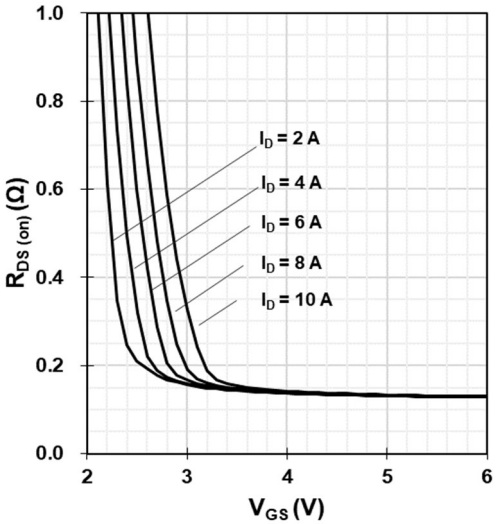
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 ºC

Figure 3 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 25 ºC

Figure 4 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 125 ºC

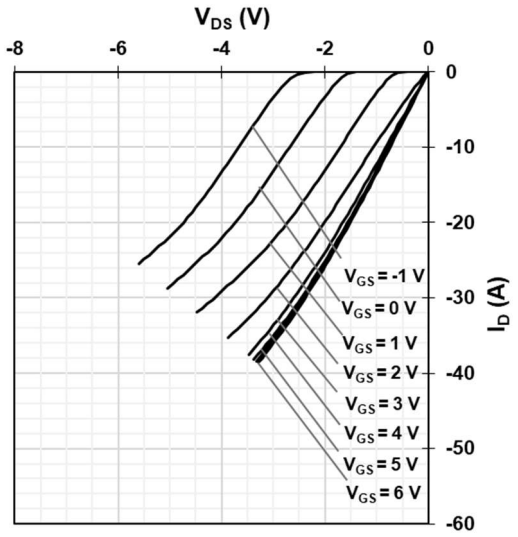
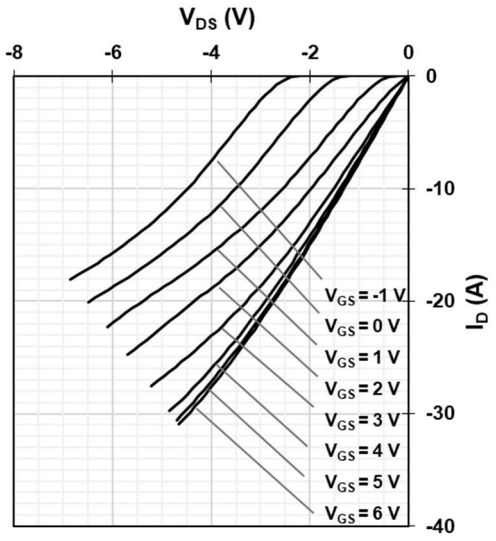
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 ºC	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 ºC

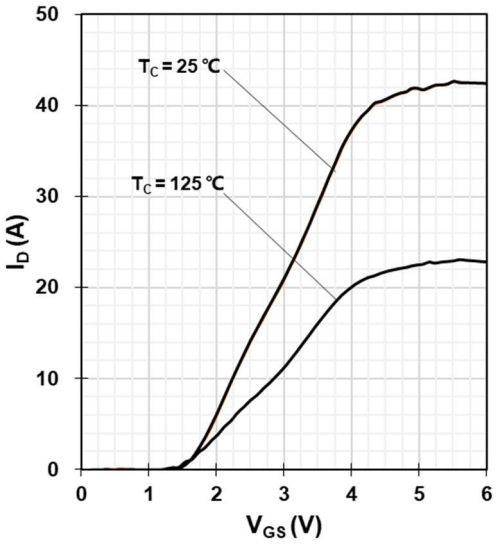
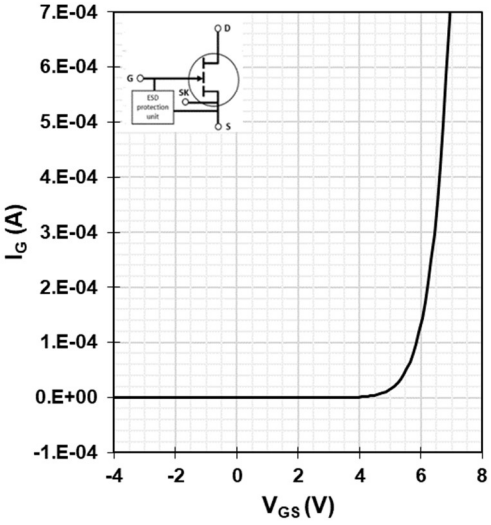
Figure 7 Typ. transfer characteristics	Figure 8 Typ. gate-to-source leakage
	
$I_D = f(V_{GS})$; V_{DS} = 5 V	$I_G = f(V_{GS})$; V_D = open

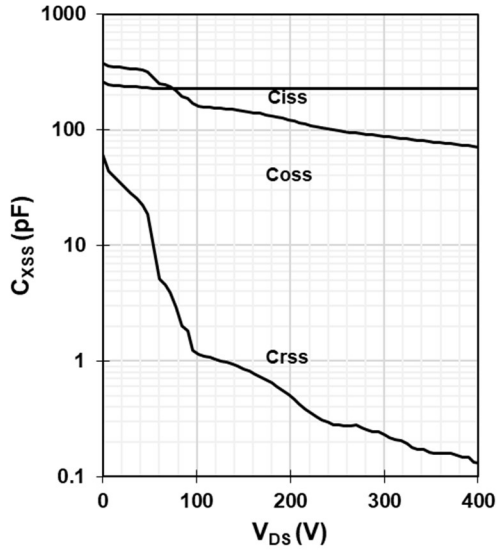
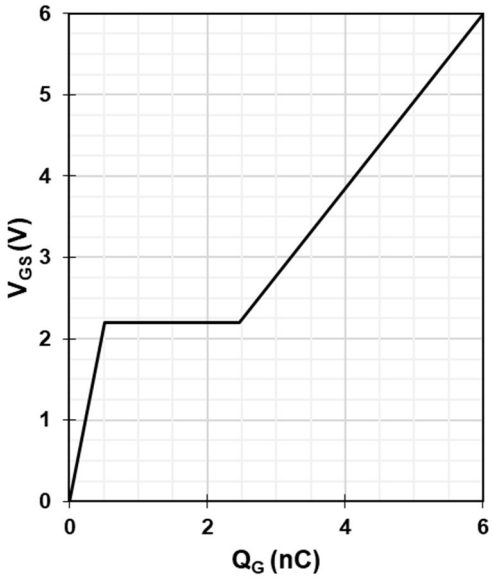
Figure 9 Typ. capacitances	Figure 10 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 100 kHz	V_{GS} = f(Q_G); $V_{DC-LINK}$ = 400 V; I_D = 8 A

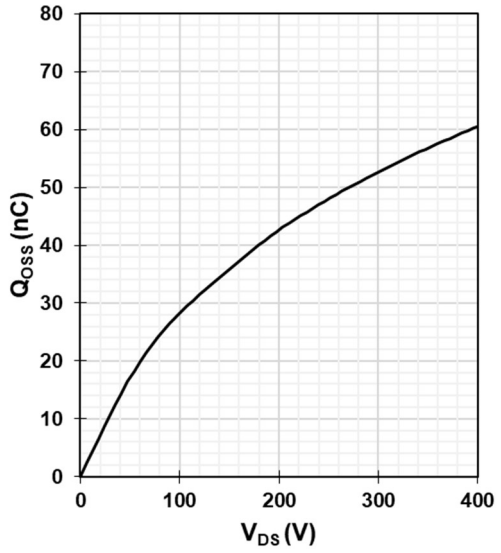
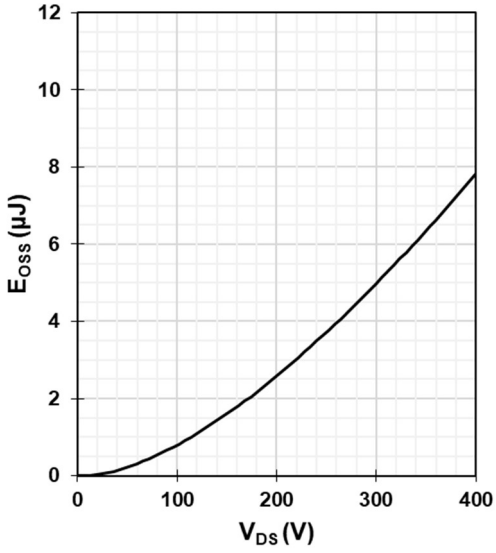
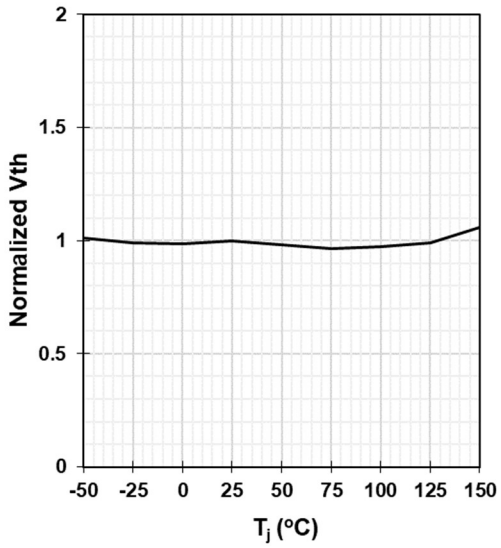
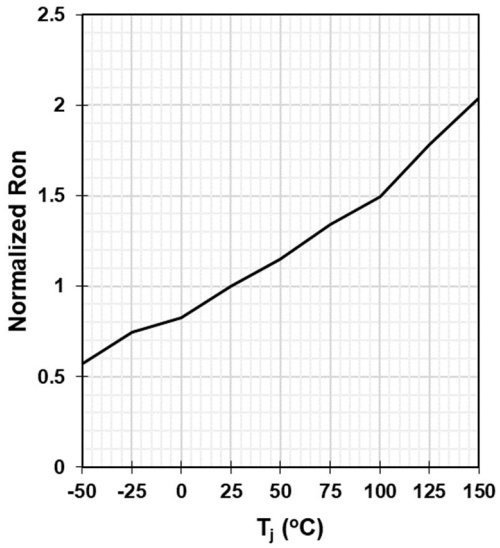
Figure 11 Typ. output charge	Figure 12 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100 kHz	E_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 13 Gate threshold voltage



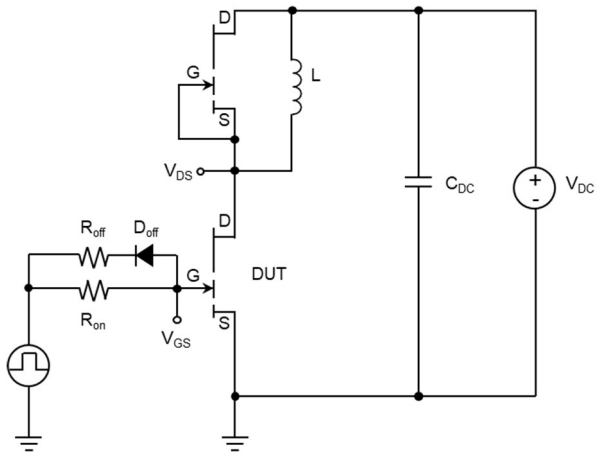
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 30 mA

Figure 14 Drain-source on-state resistance



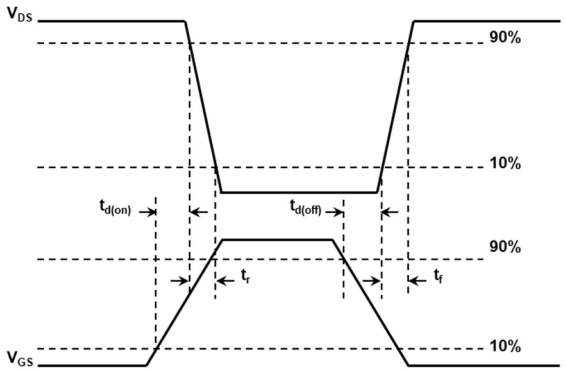
$R_{DS(on)} = f(T_j)$; I_D = 8 A; V_{GS} = 6 V

Figure 15 Switching time test circuit

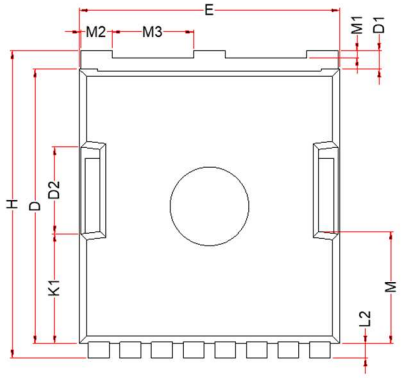


V_{DS} = 400 V, I_D = 6 A, L = 120 μH, V_{GS} = 6 V,
R_{on} = 10 Ω, R_{off} = 1 Ω

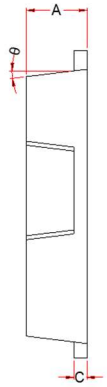
Figure 16 Typ. switching time waveform



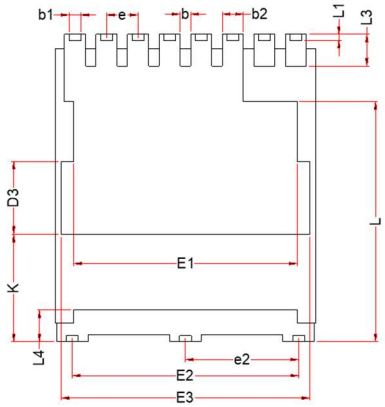
5 Package outlines



TOP VIEW



SIDE VIEW

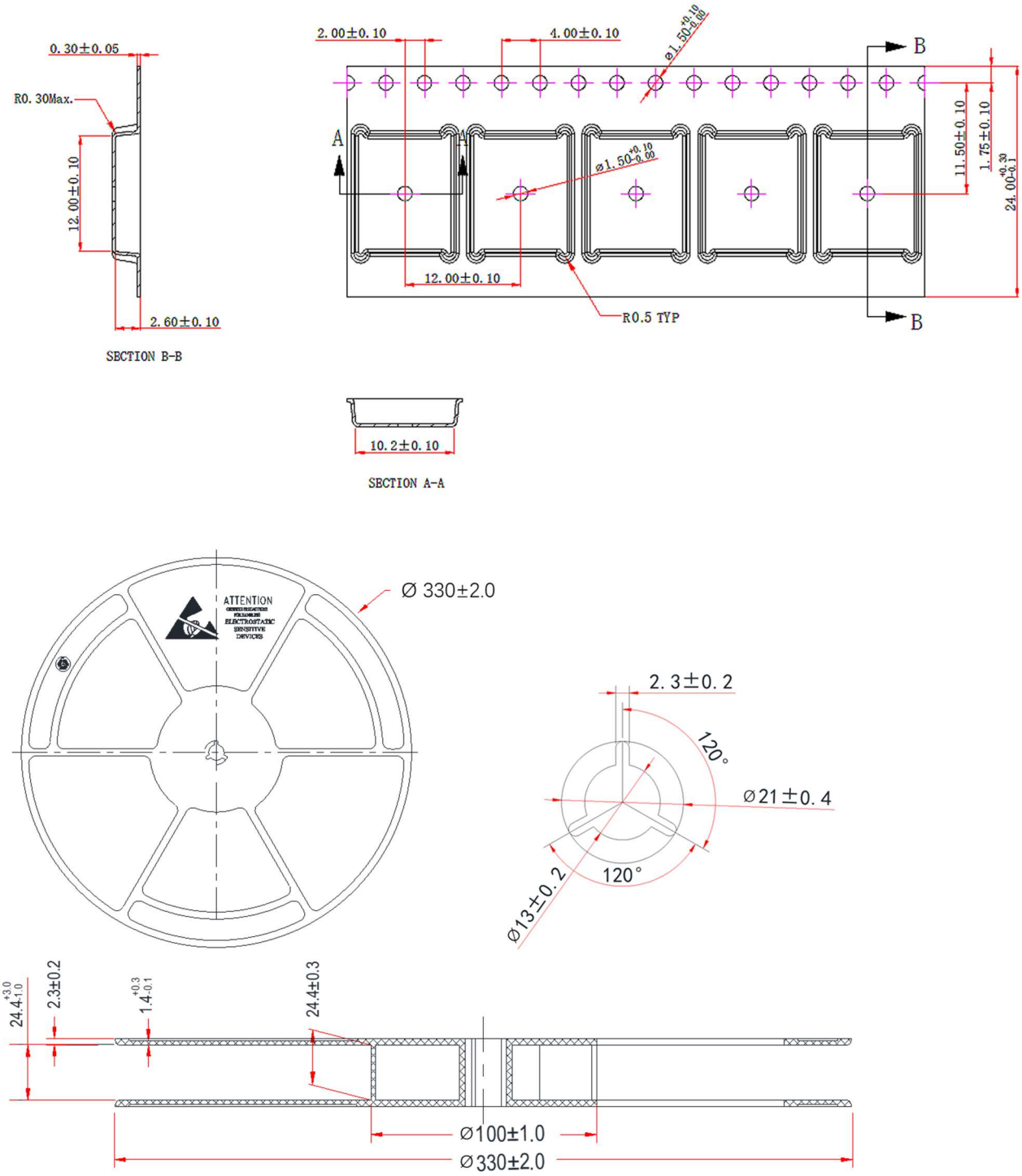


BOTTOM VIEW

Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	ASSY lot No.	XXXXXXXX
Row 3	Year & Week	YXWX

SYMBOL	MIN	MAX
A	2.20	2.40
b	0.30	0.50
b1	0.35	0.55
b2	0.70	0.90
c	0.40	0.60
D	10.28	10.58
D1	0.60	0.80
D2	(3.30)	
D3	(2.77)	
E	9.70	10.10
E1	(8.50)	
E2	(8.50)	
E3	(9.46)	
e	1.10	1.30
H	11.48	11.88
K	(4.08)	
K1	(4.17)	
L	(9.13)	
L1	0.13	0.33
L2	0.50	0.70
L3	1.10	1.30
L4	1.10	1.30
M	(4.23)	
M1	0.16	0.36
M2	1.10	1.30
M3	3.00	3.20
θ	4°	10°
e2	4.20	4.40

6 Reel information



7 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-11-23	1.0 version release