

CGD1001 Single-Channel Low-Side GaN Gate Driver

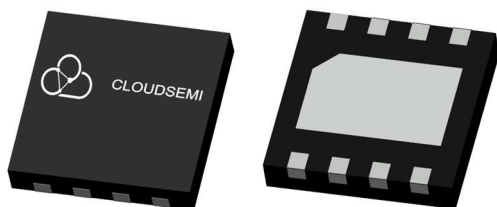
Description

CGD1001 is a single-channel gate driver IC, designed to drive GaN FETs. With strong sink current capability, CGD1001 can drive multiple GaN FETs in parallel. CGD1001 features wide logic input range with hysteresis, compatible to traditional MOSFET controller. Also, CGD1001 features wide power supply range of 10~18 V. The gate drive voltage VDD of 6V is stably provided by internal LDO, making an easier circuit design.

The integrated under-voltage lock-out (UVLO) protection feature is provided drivers to prevent GaN transistors from operating in low efficiency or dangerous conditions.

The independent SGND and PGND design can make sure a reliable logic input signal and a clean gate driving loop.

The driver operates in the temperature ranging from -40°C to +125°C. The device is available in a compact 3 x 3 mm DFN package for a minimized parasitic inductance.



Features

- Single-channel GaN gate driver IC
- Wide logic input range with hysteresis
- Wide power supply range (10 V to 18 V)
- Internal 6-V LDO for stable gate drive voltage
- Independent SGND and PGND design
- Independent source and sink outputs for controllable rise and fall time
- 4-A/2-A peak sink and source drive current
- UVLO protection
- -40°C to +125°C operating temperature range
- 8-PIN DFN3*3 package

Typical applications

- AC/DC, DC/DC, DC/AC
- Totem pole PFC, LLC
- Mobile fast-chargers, adapters
- LED lighting, Class-D audio
- Micro-inverters, energy storage systems
- TV / monitor, wireless power
- Server, telecom & networking SMPS
- Uninterruptable power supplies (UPS)

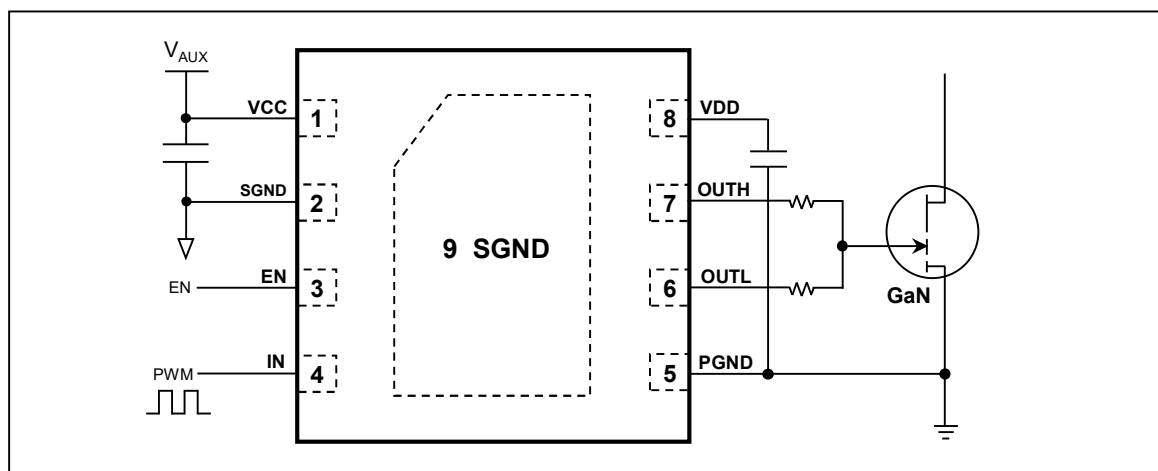


Figure 1 Typical application circuit

Pin configuration and functions

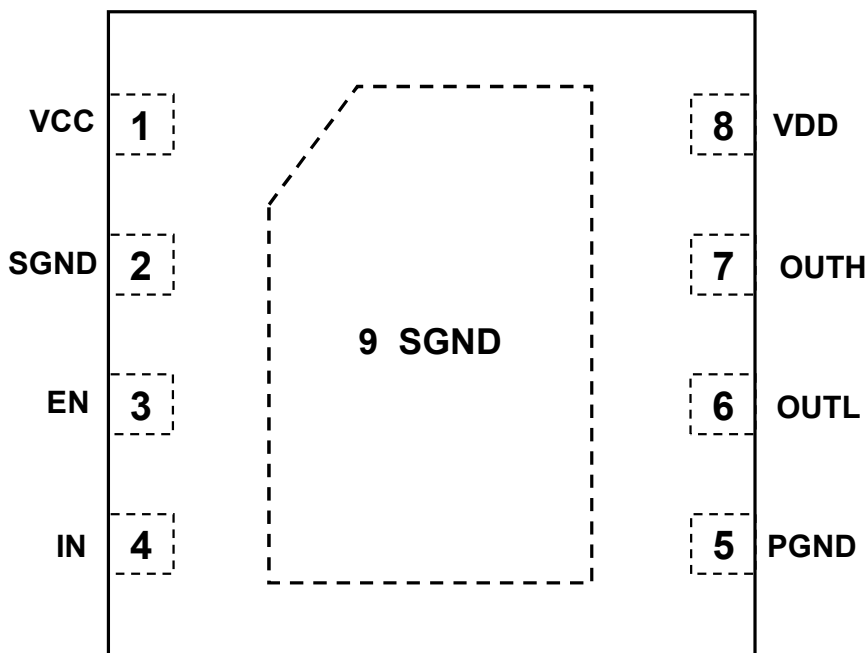


Figure 2 Package 8-PIN DFN3*3 top view

Pin #	Name	I/O	Description
1	V _{CC}	I	Gate driver supply voltage. Locally bypass this pin to SGND with a ceramic capacitor.
2	SGND	G	Logic ground
3	EN	I	Enabling signal logic input
4	IN	I	PWM signal logic input
5	PGND	G	Gate driver ground.
6	OUTL	O	Gate driver turn-off slew-rate set pin
7	OUTH	O	Gate driver turn-on slew-rate set pin
8	V _{DD}	O	6V LDO output. This pin provides power to driving stage. Locally bypass this pin to PGND with a ceramic capacitor.
9	SGND	G	Logic ground.

I = Input, O = Output, G = Ground

Ordering information

Ordering Code	Package	Marking	Packing
CGD1001	8-PIN DFN3*3	CGD1001	Reel

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1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute maximum ratings* may cause permanent damage to the device.

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V _{CC} -SGND voltage	V _{CC}	-0.3	-	24	V	
V _{DD} -PGND voltage	V _{DD}	-0.3	-	7	V	
SGND-PGND voltage	V _{SP}	-5	-	5	V	
Operating temperature	T _j	-40	-	+125	°C	
Storage temperature	T _{stg}	-55	-	+150	°C	

2 Recommended operating conditions

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V _{CC} -SGND voltage	V _{CC}	10	-	18	V	
PWM input pin voltage	V _{IN}	0	-	18	V	
Junction temperature	T _j	-40	-	+125	°C	
Ambient temperature	T _a	-40	-	+125	°C	

3 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R _{thJC}	-	-	0.9	°C/W	
Reflow soldering temperature	T _{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

Typical values represent the most likely parametric norm at $T_j = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{CC} = 12\text{ V}$

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
V _{CC} Supply Characteristics						
V _{CC} quiescent current	I _{QCC}	-	0.74	-	mA	V _{IN} = 0 V
V _{CC} operating current	I _{QCC-SW}	-	2	-	mA	F _{SW} = 500 kHz, C _{LOAD} = 100 pF
V _{CC} UVLO rising threshold	V _{CC-ON}	8.1	8.4	8.8	V	
V _{CC} UVLO falling threshold	V _{CC-OFF}	7.5	7.8	8.1	V	
V _{CC} UVLO hysteresis	V _{CC-HYS}	0.4	0.6	-	V	
Logic input Characteristics						
Input pin pull-down resistance	R _{IN-PD}	-	200	-	kΩ	H _{IN} = 3 V
Input pin high logic bias current	I _{IN-H}	-	20	-	μA	H _{IN} = 5 V
Enable pin pull-down resistance	R _{EN_PD}	-	200	-	kΩ	EN = 3 V
Enable pin high logic bias current	I _{EN_H}	-	20	-	μA	EN = 5 V
Input logic high threshold (rising edge)	V _{INH} , V _{ENH}	1.7	2.1	2.5	V	
Input logic low threshold (falling edge)	V _{INL} , V _{ENH}	0.9	1.2	1.5	V	
Input logic hysteresis	V _{IN-HYS} , V _{EN_HYS}	0.8	0.9	-	V	
Driver Output Characteristic						
Regulator Output Voltage	V _{VDD}	5.7	6	6.3	V	C _{VDD} = 100 nF
Driver output pull-down resistance	R _{SNK}	-	1	-	Ω	
Driver output pull-up resistance	R _{SRC}	-	51	-	Ω	
Output peak source current	I _{SRC_PK}	-	2	-	A	
Output peak sink current	I _{SNK_PK}	-	4	-	A	

Parameters	Symbols	Values			Units	Notes/Conditions
		Min.	Typ.	Max.		
Switching Characteristics						
Switching frequency	F _{SW}	-	-	2	MHz	
Pulse width	T _{PW}	0.02	-	1000	μs	
Turn-on propagation delay	T _{ON}	-	8.5		ns	see Figure 4
Turn-off propagation delay	T _{OFF}	-	10.7		ns	
Output rise time	T _R	-	11	-	ns	C _{LOAD} = 1 nF
Output fall time	T _F	-	5	-	ns	see Figure 4

5 Functional block diagram

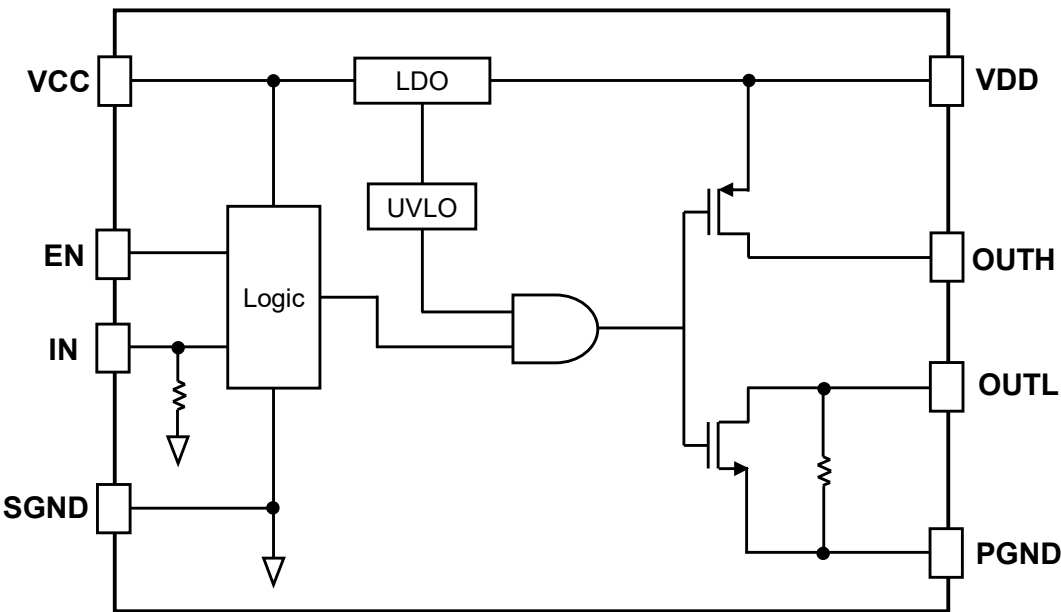


Figure 3 Functional block diagram

6 Timing diagram

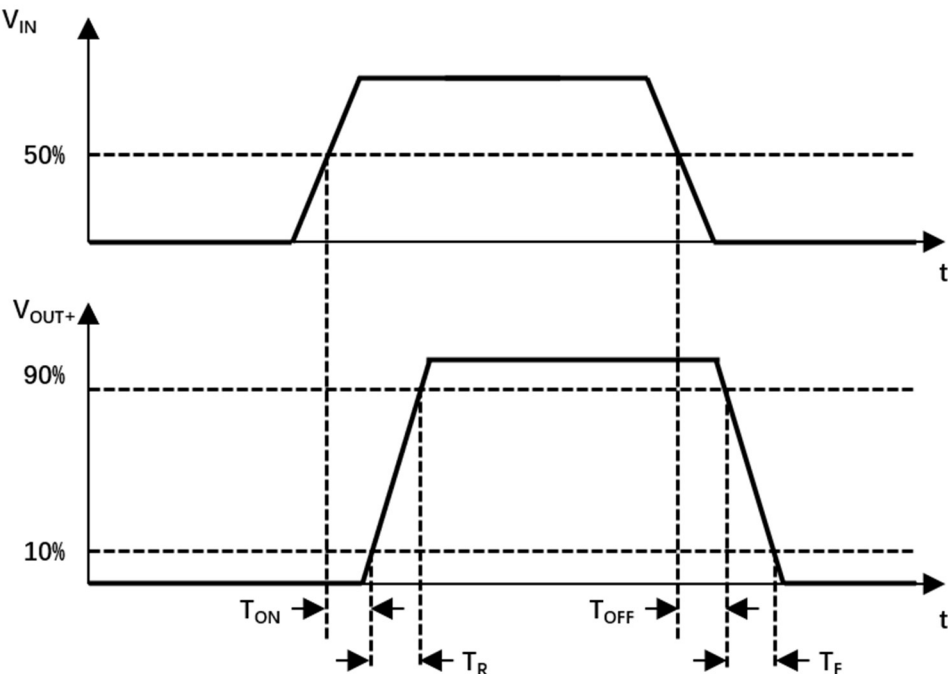
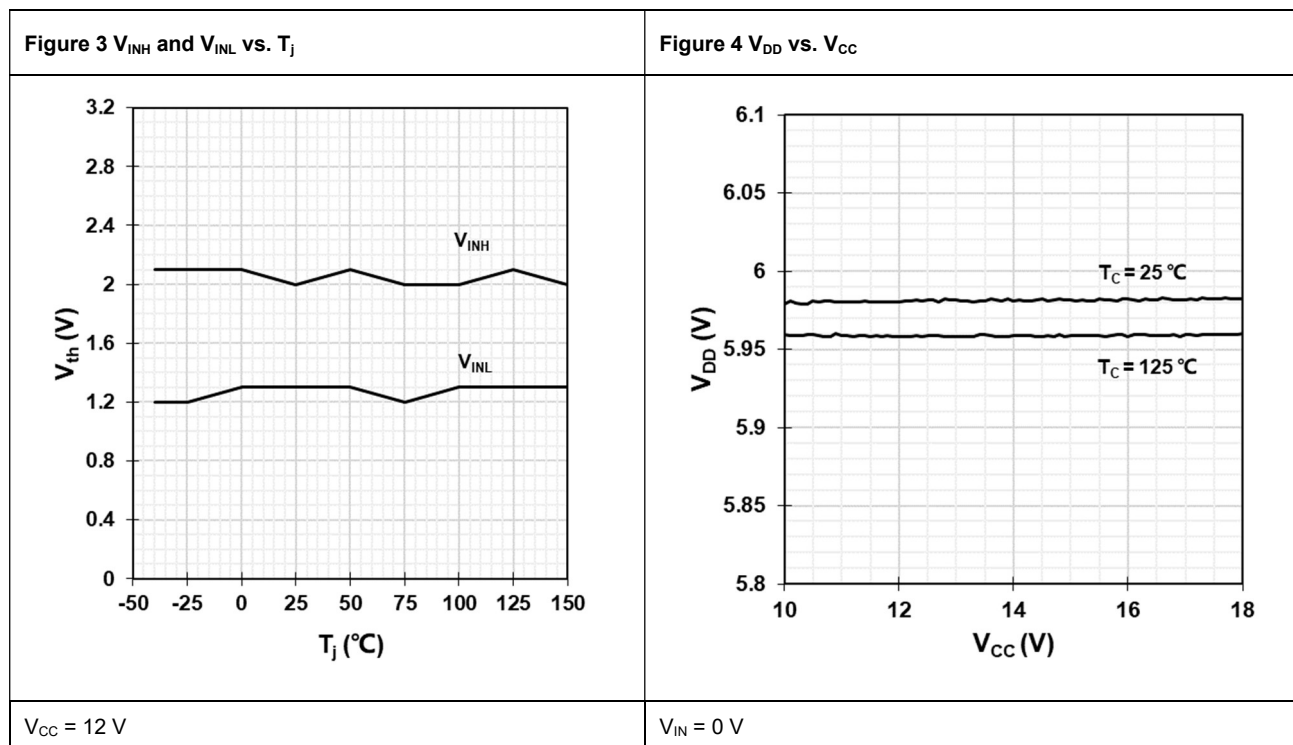
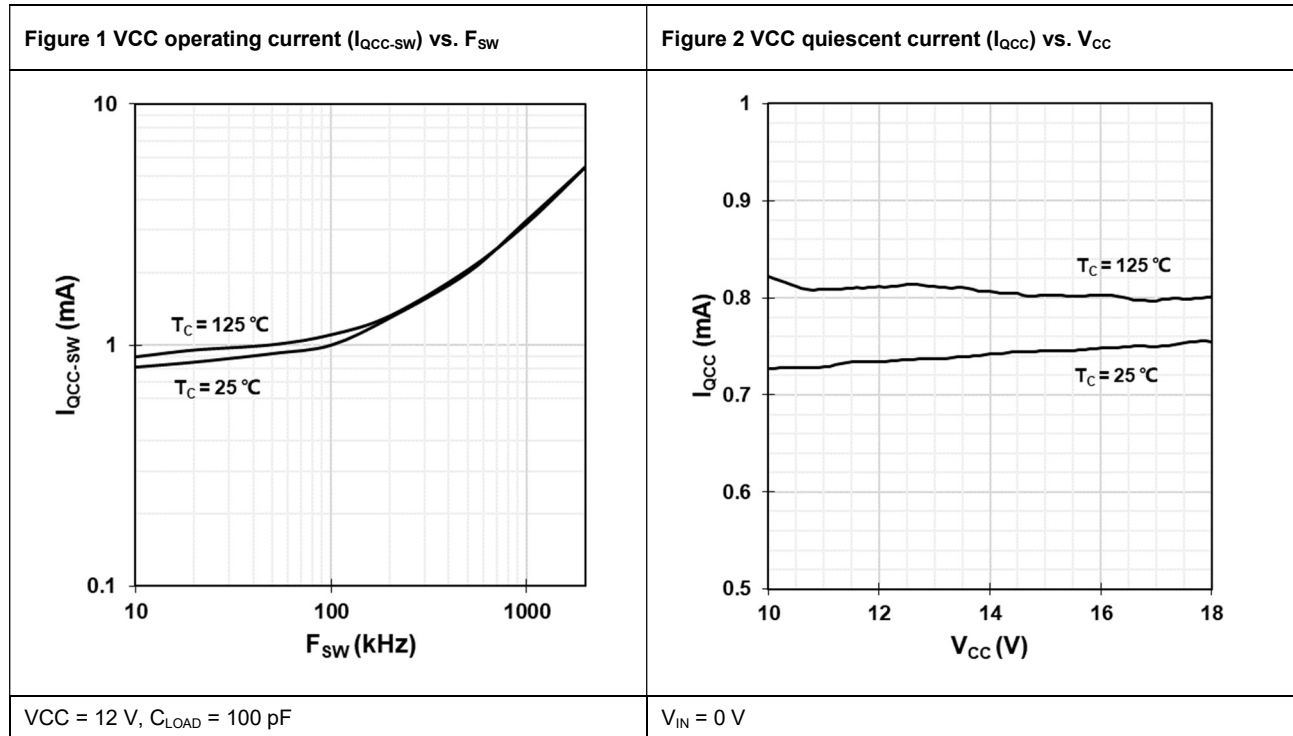


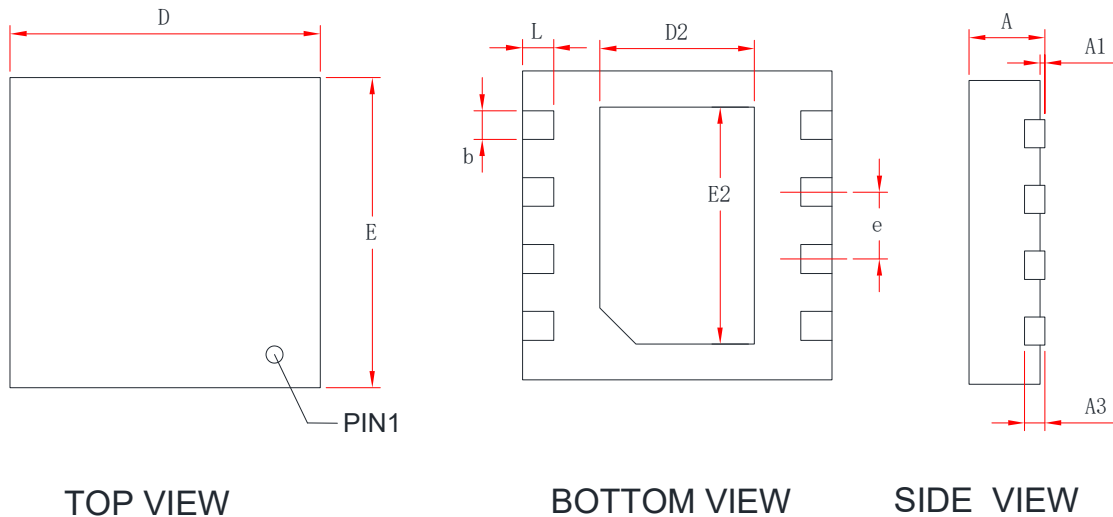
Figure 4 Propagation delay and rise/fall time definitions

7 Electrical characteristics diagrams

at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.



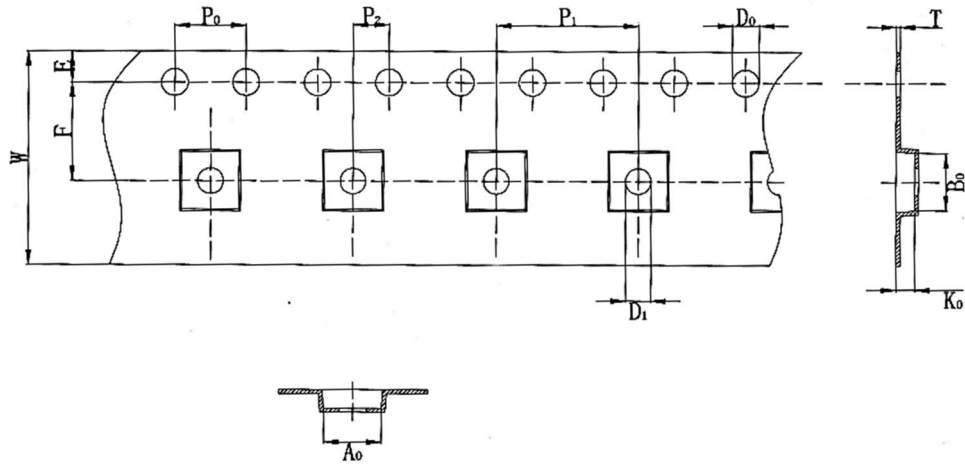
8 Package outlines



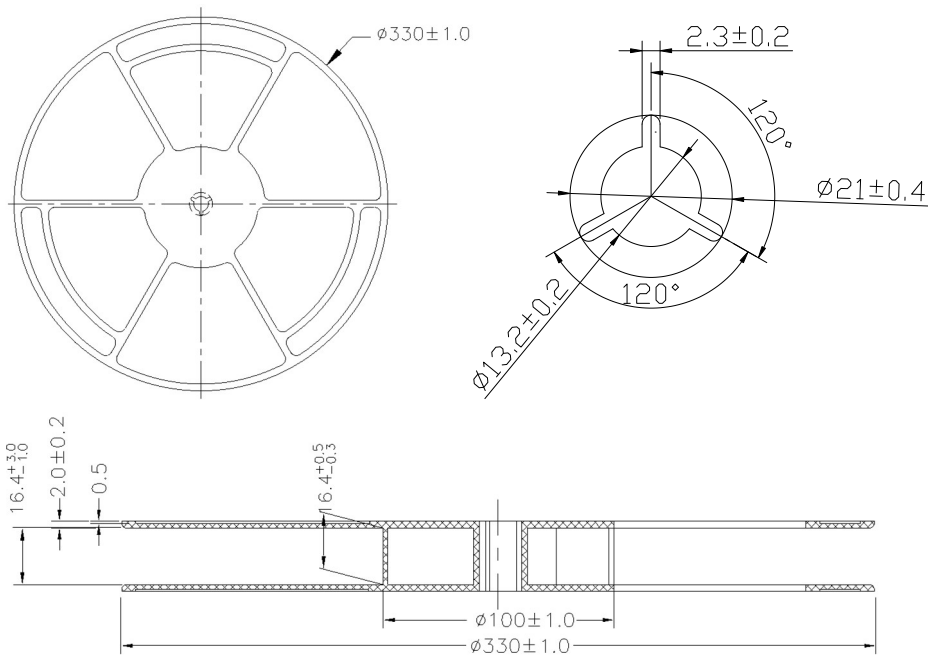
Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	ASSY lot No.	XXXXXXXX
Row 3	Year & Week	YXWX

Symbols	MIN	MID	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
A3	0.203 REF		
b	0.23	0.28	0.33
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	2.20	2.30	2.40
e	0.65 TYP		
L	0.25	0.3	0.35

9 Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	12.00±0.20	10P0	40.00±0.20
E	1.75±0.10	P1	8.00±0.10
F	5.50±0.10	A0	3.23±0.10
D0	1.50±0.10	B0	3.23±0.10
D1	1.50±0.10	K0	1.05±0.10
P0	4.00±0.10	T	0.23±0.05
P2	2.00±0.05		



10 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-5-31	1.0 version release