# Low-side Gate Driver for Normally-OFF GaN FET

## General description

The CGD1003 is a single channel low-side enhancement-mode GaN FET and logic-level MOSFET driver for high switching frequency applications, including LiDAR, Time-of-Flight (ToF), and power converter. The very fast switching frequency combined with the ultra-narrow pulse width significantly enhance the LiDAR and ToF performance. The minimum 1-ns input pulse width makes higher power/current allowable in these applications to improve mapping range and resolution. The extremely small propagation delay of 3.3ns significantly improves the control loop response time and thus overall performance of the power converters. Split output allows the drive strength and rise/fall time to be independently adjusted through external resistors between OUTH, OUTL, and the FET gate.

CGD1003 features undervoltage lockout (UVLO) and over-temperature protection (OTP) to ensure the device is not damaged in overload or fault conditions.

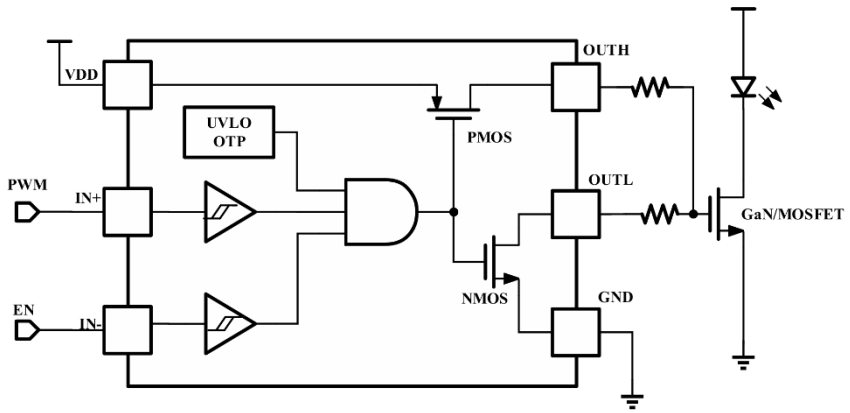
CGD1003 is available in 2mm*2mm DFN package with Wettable Flank Plated (WFDFN) to meet the size and gate loop inductance requirements for high-speed switching applications.

## Features

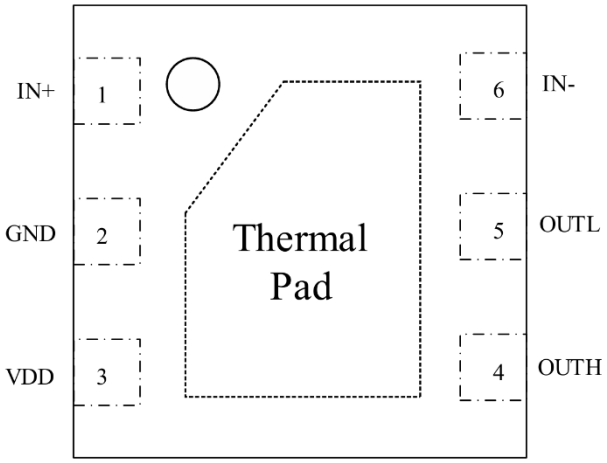
- AEC-Q100 grade 1 qualified
- 1.25-ns typical minimum input pulse width (220-pF load)
- 3.3-ns typical rising/falling propagation delay
- Up to 100-MHz Operation
- 7-A pull-up and 5-A pull-down current
- 650-ps typical rise/fall time (220-pF load)
- 2-mm x 2-mm DFN package with Wettable Flank Plated (WFDFN)
- Inverting and non-inverting inputs
- UVLO and over-temperature protection
- Recommended single 5-V supply voltage

## Typical applications

- Automotive LiDAR
- Vehicle Occupant Detection Sensor
- Class-E Wireless Charger
- GaN-Based Synchronous Rectifier



## Pin configuration and functions




**2mm*2mm WFDFN TOP VIEW**

| Pin # | Name | I/O [1] | Description |
|---|---|---|---|
| 2 | GND | G | Connect with a direct path to the transistor source. |
| 1 | IN+ | I | Positive logic-level input. |
| 6 | IN- | I | Negative logic-level input. |
| 5 | OUTL | O | Pull-down gate drive output. Connect through an optional resistor to the target transistor gate. |
| 4 | OUTH | O | Pull-up gate drive output. |
| 3 | VDD | P | Input voltage supply. Decouple through a compact capacitor to GND. |
| | thermal | | Internally connected to GND through substrate. |

*1. I = Input, O = Output, P = Power, G = Ground, NC = No Connect*

# Table of Contents

# 1 Absolute maximum ratings

At $T_j$ = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate product lifetime. For further information, contact CloudSemi sales office.

| Symbols | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| VDD | Supply voltage | 0 | 5.75 | V |
| VIN | IN+ or IN- input voltage | -0.3 | 6 | V |
| VOUT | OUTH, OUTL pin voltage | -0.3 | 6 | V |
| $T_J$ | Operating temperature | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature | -55 | 150 | °C |

# 2 Recommended operating conditions

| Symbols | Parameters | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| VIN | IN+ or IN- input voltage | 0 | | $V_{DD}$ | V |
| VOUT | OUTH, OUTL pin voltage | -5 | | $V_{DD}$ | V |
| $T_J$ | Operating Temperature | -40 | | 125 | °C |

# 3 Thermal characteristics

| Symbols | Parameters | Values | Units |
|---|---|---|---|
| $R_{th(J-A)}$ | Thermal resistance junction-to-ambient | 67 | °C/W |

# 4 ESD ratings

| Parameters | Symbols | Values | Units |
|---|---|---|---|
| V(ESD) Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | ±500 | V |
| | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins | ±2000 | V |

# 5 Electrical characteristics

## 5.1 Static characteristics

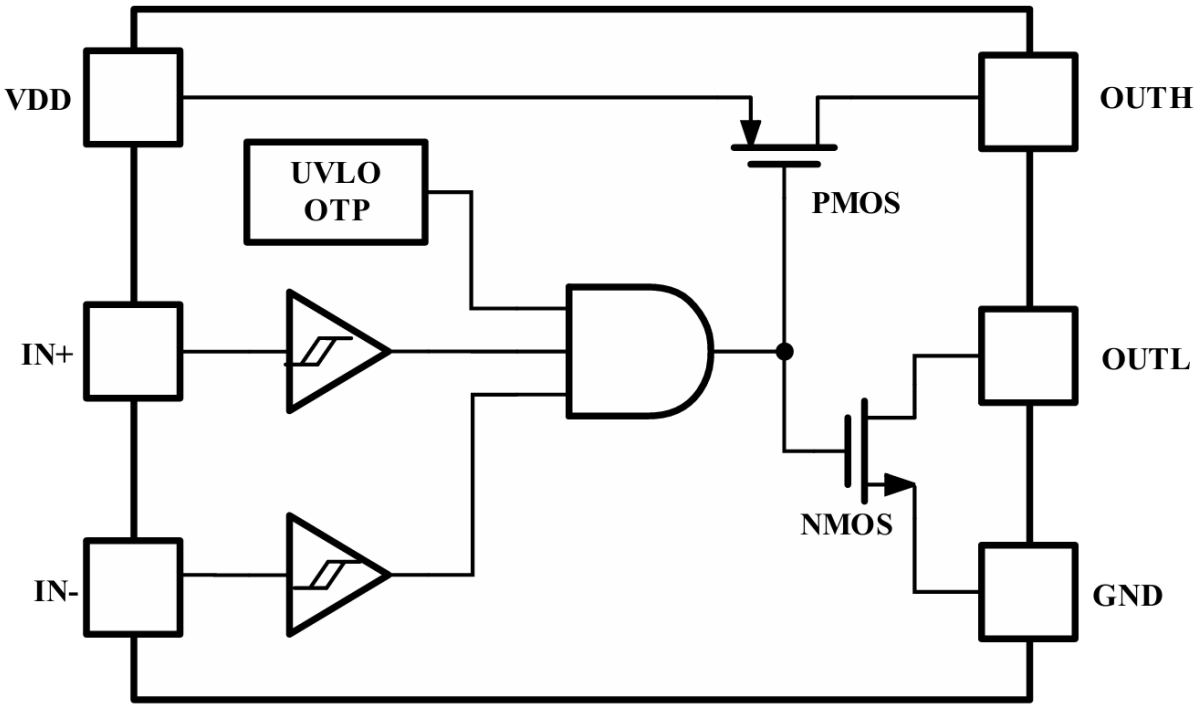
| Symbols | Parameters | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | |
| $I_{VDD,q}$ | VDD Quiescent Current | 64 | 88 | 128 | μA | IN+ = IN- = 0V |
| $I_{VDD,op}$ | VDD Operating Current | | 5 | | mA | $f_{sw}$=1MHz, $C_L$=330pF |
| | | | 383 | | | $f_{sw}$=100MHz, $C_L$=330pF |
| $V_{DD,UVLO}$ | Under-voltage Lockout | 3.9 | 4.1 | 4.2 | V | $V_{DD}$ rising |
| $V_{DD,UVLO\_HYS}$ | UVLO Hysteresis | | 200 | | mV | |
| $T_{OTP}$ | Over temperature shutdown turn-off threshold | | 164 | | °C | |
| $T_{OTP\_HYS}$ | Over temperature hysteresis | | 20 | | °C | |
| **Input DC Characteristics** | | | | | | |
| $V_{IH}$ | IN+, IN- high threshold | 1.6 | | 2.5 | V | |
| $V_{IL}$ | IN+, IN- low threshold | 1.1 | | 1.9 | V | |
| $V_{IHYS}$ | IN+, IN- hysteresis | 0.4 | | 0.9 | V | |
| $R_{IN+}$ | Positive input pull-down resistance | 100 | 180 | 200 | kΩ | To GND |
| $R_{IN-}$ | Negative input pull-down resistance | 100 | 180 | 200 | kΩ | To GND |
| **Output DC Characteristics** | | | | | | |
| $I_{OH}$ | Peak source current | | 7 | | A | |
| $I_{OL}$ | Peak sink current | | 5 | | A | |

## 5.2 Switching characteristics

| Symbols | Parameters | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{start}$ | Startup Time, $V_{DD}$ rising above UVLO | 40 | 50 | 70 | us | IN- = GND, IN+= $V_{DD}$, $V_{DD}$ rising above 4.4V to OUTH rising |
| $t_{pd,r}$ | Propagation delay, turn on | 2 | 3.3 | 4 | ns | IN- = 0V, IN+ to OUTH, 220-pF load |
| $t_{pd,f}$ | Propagation delay, turn off | 2 | 3.3 | 4 | ns | IN- = 0V, IN+ to OUTL, 220-pF load |
| $t_{rise}$ | Output rise time | | 650 | | ps | 0Ω series 220pF load [1] |
| $t_{fall}$ | Output fall time | | 650 | | ps | 0Ω series 220pF load [1] |
| $t_{min}$ | Minimum input pulse width | | 1.25 | | ns | 0Ω series 220pF load [1] |

*1. Rise and fall time calculated as time from 20% of the gate voltage to 80% of the gate voltage of the GaN FET.*

# 6 Block diagram




# 7 Function description

## 7.1 Input stage

The input stage features two Schmitt-triggers at the pins IN+ and IN- to reduce sensitivity to noise on the inputs. IN+ is connected with a pull-down resistor while IN- is connected with a pull-up resistor to prevent unintended turn-on. The output of the driver will be high when input voltage goes above input thresholds and output goes low when input voltage is below input threshold mentioned in the electrical characteristics table. Both IN+ and IN- are single ended inputs, and these two pins cannot be used as a differential input pair. Parasitic elements become extremely important in high frequency designs and extreme care should be taken while laying out the printed circuit board to minimize these parasitic elements. The performance of the CGD1003 and the performance of the overall system gets affected by the layout and components being selected.

## 7.2 Output stage

CGD1003 provides 7-A source, 5-A sink (asymmetrical drive) peak-drive current capability, and features a split output configuration. The OUTH and OUTL outputs of the CGD1003 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turn-on and turn-off drive strengths to control slew rate and EMI, and to control ringing on the gate signal.

The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device Ciss, and thus preventing false turn-on. This ringing heavily depends on the layout as switching frequency increases and as rise and fall time gets shorter. The distance between the gate driver and power device needs to be as minimum as possible.

## 7.3 Bias Supply and Under Voltage Lockout

CGD1003 also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.0 V and 4.35 V with a hysteresis of 200mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low RDS(ON) region. During UVLO condition, the OUTL pin is pulled down to ground.

## 7.4 Overtemperature Protection (OTP)

CGD1003 features overtemperature protection (OTP) function by having a rising edge trigger point at around 164°C of junction temperature. With a hysteresis of 20°C, the device can restart to operate when junction temperature is below 144°C.

## 7.5 Truth table

| IN- | IN+ | OUTH | OUTL |
|---|---|---|---|
| L | L | OPEN | L |
| L | H | H | OPEN |
| H | L | OPEN | L |
| H | H | OPEN | L |

## 7.6 Typical testing waveforms

CGD1003 can be used to drive pulses of nano seconds duration on to a capacitive load. CGD1003 can be driven with an equivalently short pulse on one input pin. However, this takes a sufficiently strong digital driver and careful consideration of the routing parasitic from digital output to input of CGD1003. Two inputs and included AND gate in CGD1003 provide an alternate method to create a short pulse at the CGD1003 output. Starting with both IN+ and IN- at low, taking IN+ high will cause the output to go high. Now if IN- is taken high as well, output will be pulled low. So a digital signal and its delayed version can be applied to IN+ and IN- respectively to create a pulse at the output with width corresponding to the delay between the signals, as shown in Figure 1. The delay can be digitally controlled in the nanosecond range.

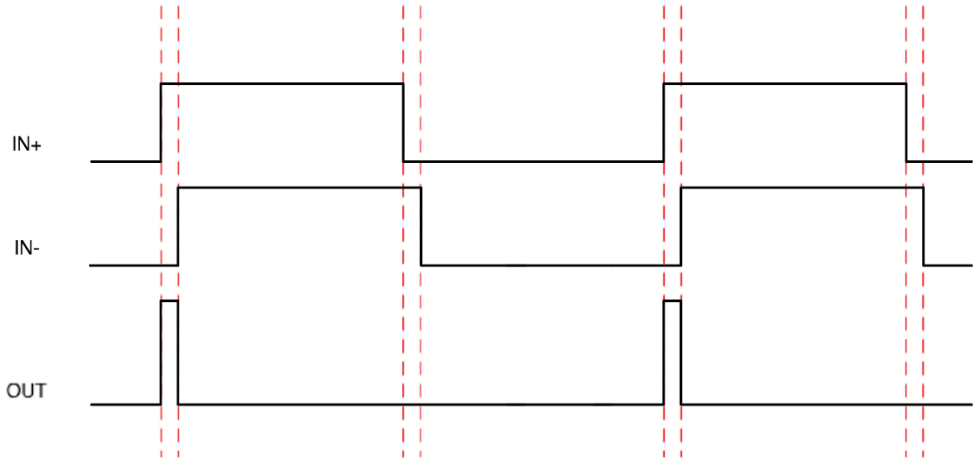



Figure 1. Timing diagram to create short pulses

If a separate delayed version of the digital signal is not available, an RC delay followed by a buffer can be used to derive the second signal, as shown in Figure 2.

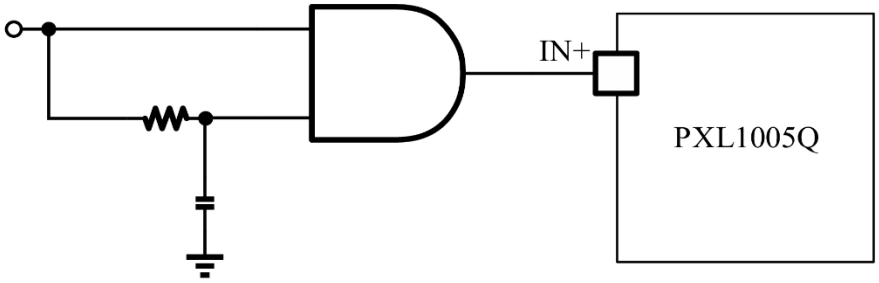
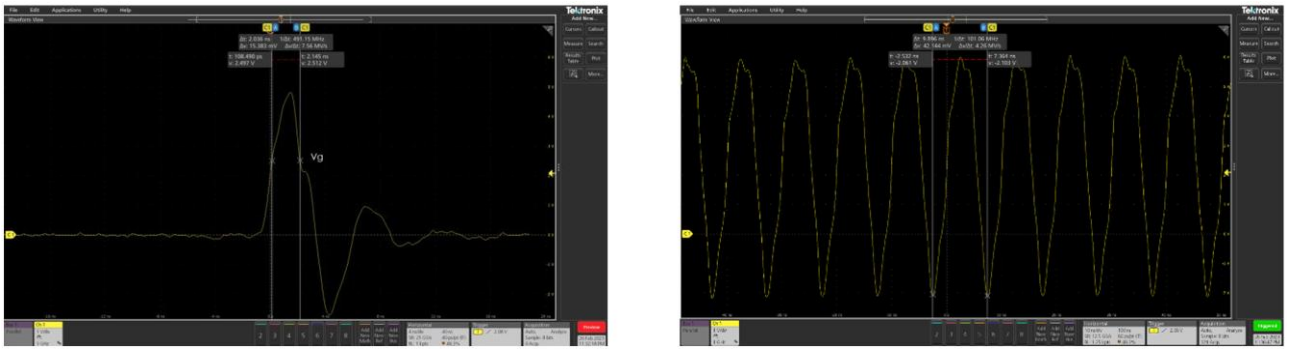



Figure 2. Single buffer and RC to create short pulses



(Left) 1.2-ns input pulse yielding 2ns output pulse (GaN device: EPC2212); (Right) 100MHz output pulse (GaN device: EPC2212)

## 8 Layout guidelines

The layout of the CGD1003 is critical to its performance and functionality. The CGD1003 is available in a WFQFN 2*2 package, which enables low-inductance connection to a BGA-type GaN FET. Figure 3 shows the recommended layout of the CGD1003 with a ball-grid array GaN FET.

A four-layer or higher layer count board is required to reduce the parasitic inductance of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

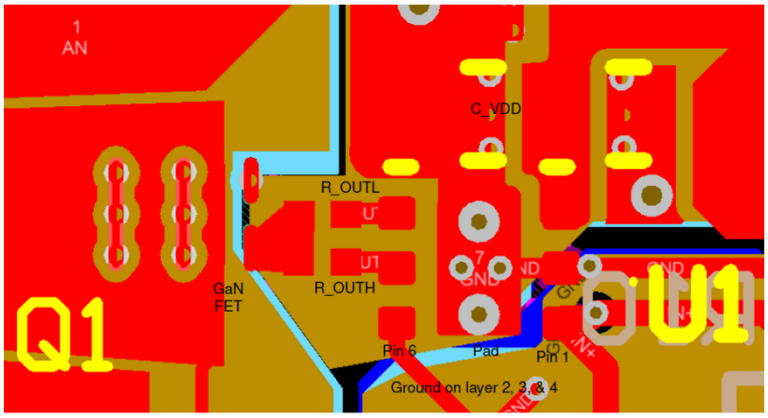



Figure 3. Layout example

## 1. Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the CGD1003. The CGD1003 should be placed as close to the GaN FET as possible, with gate drive resistors R1 and R2 immediately connecting OUTH and OUTL to the FET gate. Large traces must be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer-2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the CGD1003 GND pin connect to this plane with minimal impedance. Finally, take care to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

## 2. Bypass Capacitor

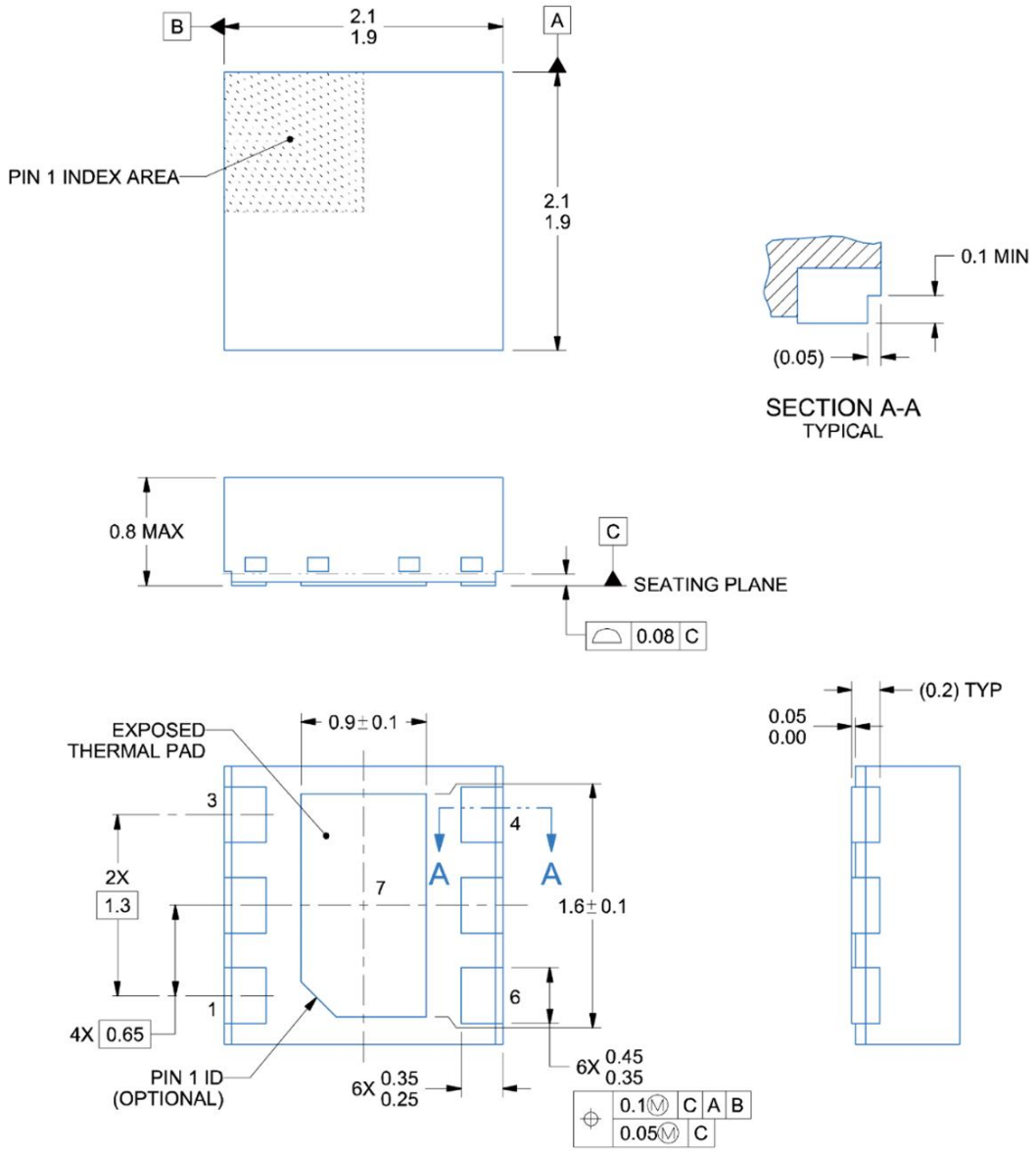
The $V_{DD}$ power terminal of the CGD1003 must by bypassed to ground immediately adjacent to the IC. Because of the fast gate drive of the IC, the placement and value of the bypass capacitor is critical. The bypass capacitor must be place on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1μF, up to 1μF, with temperature coefficient X7R or better. Recommended body types are Low Inductance Chip Capacitor (LICC), Inter-Digitated Capacitor (IDC), Feed-through, and LGA. Finally, an additional 1 nF capacitor must be placed as close to CGD1003 as practical.

# 9 Package information

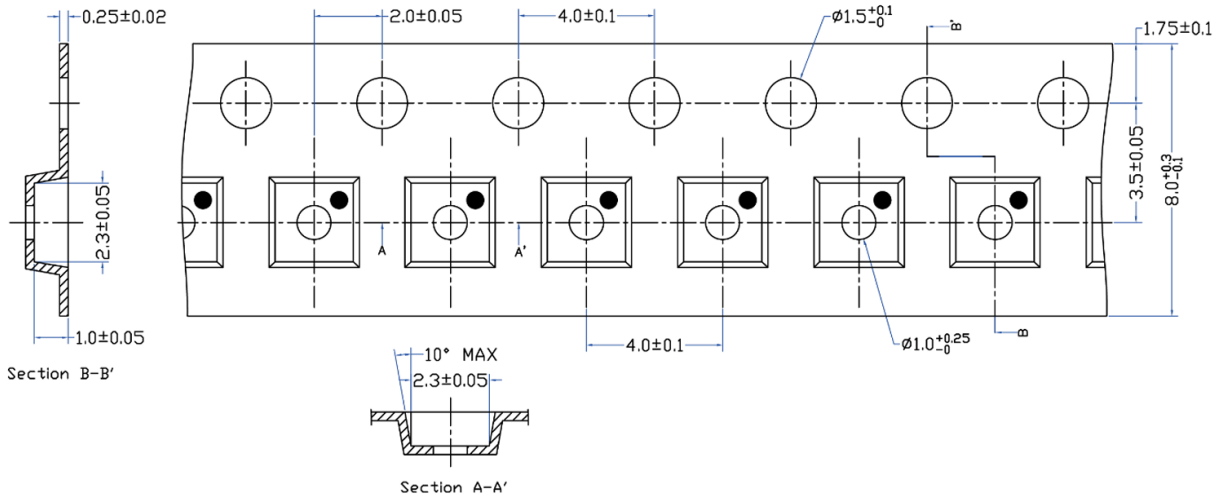
| Orderable Device | Package Type | Op Temp (°C) | Eco Plan | Package Marking | Packing Option |
|---|---|---|---|---|---|
| CGD1003 | WFDFN | -40 to 125 | RoHS & PAHs | CGD<br>XXXXX<br>XXXXXXX<br>XXX | Tape and reel,<br>3000pcs/reel |

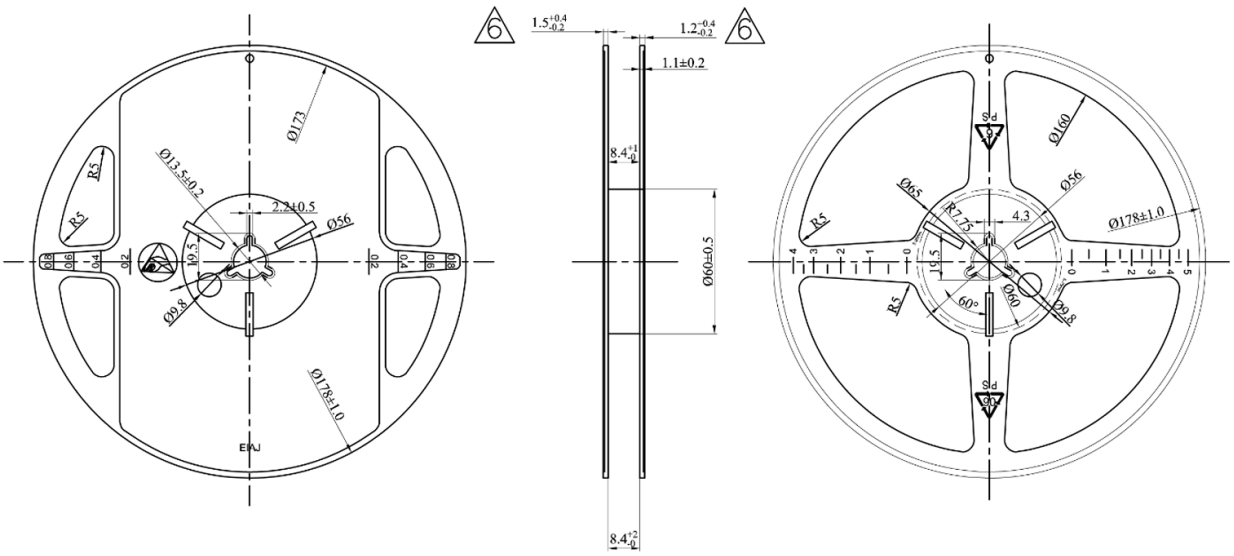
*RoHS: PowerX defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances.*

*PAHs: PowerX defines "PAHs" to mean semiconductor products that are compliant with the current EU PAHs requirements for 18 PAHs substances.*



# 10 Tape and reel information



# 11 Revision history

Major changes since the last revision

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 2025-6-5 | 1.0 version release |