Half-Bridge GaN Gate Driver with Integrated Bootstrap Diode

General description

The CGD2101WL is designed to drive both the high-side and the low-side enhancement-mode (E-mode) GaN FETs in a synchronous buck, boost, half-bridge or full-bridge configuration. The driver has an integrated 100-V bootstrap diode and independent inputs for the high-side and low-side outputs for maximum control flexibility. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of E-mode GaN FETs. The inputs of the CGD2101WL are TTL logic compatible and can withstand input voltages up to 15 V regardless of the VDD voltage. The CGD2101WL has split-gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently.

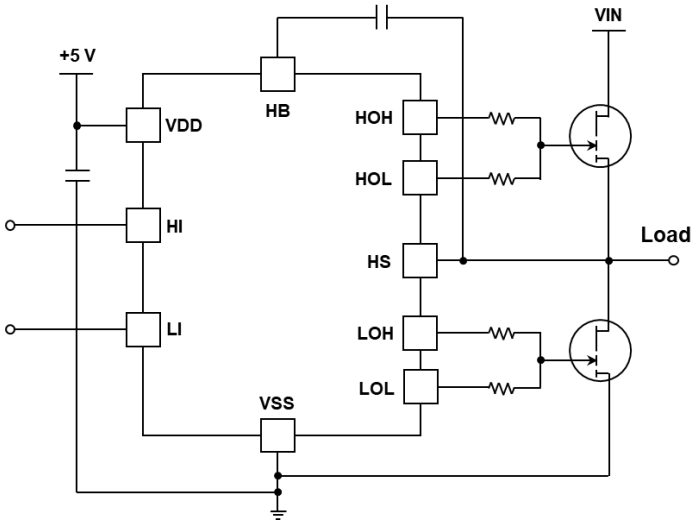
The CGD2101WL features fast propagation times and excellent minimum input pulse to ensure high-frequency applications. The CGD2101WL is available in a 12-pin WLCSP package that offers a compact footprint and minimized package inductance.

Features

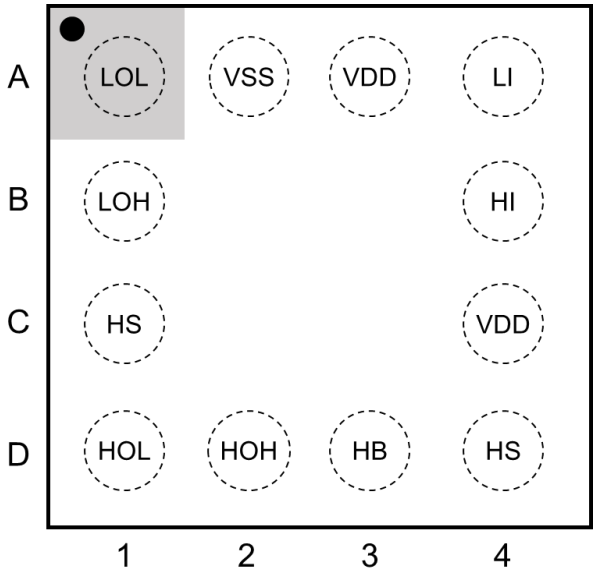
- Independent high-side and low-side TTL logic Inputs
- 1.2-A peak source, 5-A sink current
- High-side floating bias voltage rail operates up to 100 VDC
- Split outputs for adjustable turn-on, turn-off strength
- Fast propagation times (8-ns typical)
- Excellent minimum input pulse (8-ns typical)
- UVLO and over-temperature protection
- Single 5-V supply voltage
- WLCSP package with low parasitic inductance

Typical applications

- Half and full-bridge converters
- Synchronous buck converters
- Motor drive
- Class-D audio amplifiers



Pin configuration and functions



Pin #	Name	I/O [2]	Description
A1	LOL	O	Low-side gate driver sink-current output: connect to the gate of low-side GaN FET. A gate resistor can be used to adjust the turn-off speed.
A2	VSS	G	Ground return: all signals are referenced to this ground.
A3, C4 [1]	VDD	P	5-V positive gate drive supply: locally decouple to VSS using low ESR/ESL capacitor located as close as possible to the IC.
A4	LI	I	Low-side driver control input.
B1	LOH	O	Low-side gate driver source-current output: connect to the gate of low-side GaN FET. A gate resistor can be used to adjust the turn-on speed.
B4	HI	I	High-side driver control input.
C1, D4 [1]	HS	P	High-side GaN FET source connection: connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET.
D1	HOL	O	High-side gate driver turn-off output: connect to the gate of high-side GaN FET. A gate resistor can be used to adjust the turn-off speed.
D2	HOH	O	High-side gate driver turn-on output: connect to the gate of high-side GaN FET. A gate resistor can be used to adjust the turn-on speed.
D3	HB	P	High-side gate driver bootstrap rail: connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor must be placed as close as possible to the IC.

1. A3 and C4, C1 and D4 are internally connected.

2. I = Input, O = Output, P = Power, G = Ground, NC = No Connect

Table of Contents

1 Absolute maximum ratings

At T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate product lifetime. For further information, contact CloudSemi sales office.

Symbols	Parameters	Min.	Max.	Units
VDD to VSS	Driver supply voltage	-0.3	6	V
HB to HS	High-side bootstrap Voltage	-0.3	6	V
LI or HI input	Input signal voltage	-0.3	18	V
LOH, LOL output	Low-side driver output voltage	-0.3	VDD + 0.3	V
HOH, HOL output	High-side driver output voltage	VHS - 0.3	VHB + 0.3	V
HS to VSS	High-side common-mode voltage	-5	100	V
HB to VSS	Bootstrap voltage	0	106	V
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature	-55	150	°C

2 Recommended operating conditions

Symbols	Parameters	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	4.75	5	5.25	V
LI or HI INPUT	Input voltage	0	5	15	V
HS	High Side GaN Source	-5		90	V
HB	High Side GaN Gate	VHS + 4		VHS + 5.5	V
T_J	Operating Temperature	-40		125	°C

3 Thermal characteristics

Symbols	Parameters	Values	Units
$R_{th(J-A)}$	Thermal resistance junction-to-ambient	77	°C/W

4 ESD ratings

Parameters	Symbols	Values	Units
V(ESD) Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±1500	V

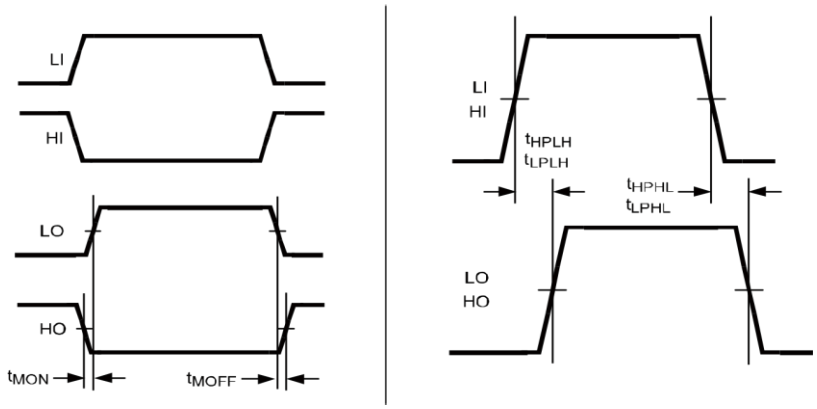
5 Electrical characteristics

5.1 Static characteristics

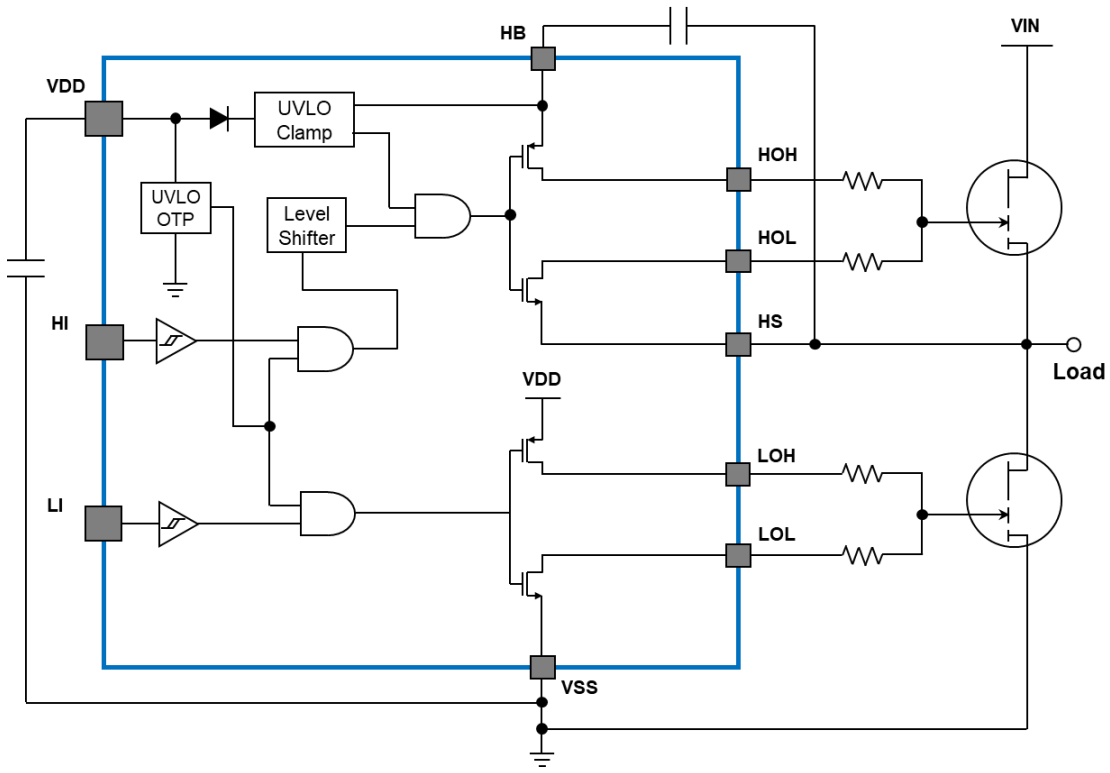
Symbols	Parameters	Min.	Typ.	Max.	Units	Test Conditions
DC Characteristics						
$I_{VDD,q}$	V_{DD} quiescent current	0.025	0.04	0.055	mA	HI = LI = 0V V_{DD} = V_{HB} = 5V
$I_{VDD,op}$	V_{DD} operating current		0.5	1	mA	fsw= 500kHz
$I_{HB,q}$	HB quiescent current	0.010	0.012	0.020	mA	HI = LI = 0V V_{DD}= V_{HB}= 5V
$I_{HB,op}$	HB operating current		0.5	1	mA	fsw= 500kHz
I_{HBS}	HB to VSS quiescent current		0.2	50	uA	HS= HB= 80V
$V_{DD,UVLO}$	V_{DD} rising threshold	3.9	4	4.2	V	V_{DD} rising
$V_{DDH,UVLO}$	V_{DD} threshold hysteresis		200		mV	
$V_{HB,UVLO}$	HB rising threshold	2.5		3.5	V	
$V_{HBH,UVLO}$	HB threshold hysteresis		200		mV	
T_{OTP}	Over temperature shutdown turn-off threshold		164		ºC	
T_{OTP}	Over temperature hysteresis		20		ºC	
Bootstrap Diode and Clamp						
V_{DL}	Low-current forward voltage	0.1	0.38	0.57	V	I_{VDD-HB} = 100uA
V_{DH}	High-current forward voltage	0.87	1	1.08	V	I_{VDD-HB} = 100mA
HB-HS clamp regulation voltage		4.5	5	5.5	V	
Input DC Characteristics						
V_{IR}	HI, LI high threshold	1.8		2.2	V	
V_{IF}	HI, LI low threshold	1.5		1.8	V	
V_{IHYS}	HI, LI hysteresis	0.4		0.9	V	
R_{IN+}	Positive input pull-down resistance	100	200	300	kΩ	To GND
Output DC Characteristics						
V_{OL}	Low-level output voltage	0.02	0.03	0.04	V	I_{HOL}= I_{LOL}= 100mA
V_{OH}	High-level output voltage V_{OH}=V_{DD}–LOH or V_{OH}=HB–HOH	0.1	0.14	0.16	V	I_{HOH}= I_{LOH}= 100mA
I_{OH}	Peak source current	1.6	1.7	1.8	A	HOH, LOH = 0 V
I_{OL}	Peak sink current	4	5	5.5	A	HOL, LOL= 5 V

5.2 Switching characteristics

Symbols	Parameters	Min.	Typ.	Max.	Units	Test Conditions
t_{start}	Startup Time, VDD rising above UVLO	40	50	70	us	LI = V_{DD}, HI = GND, V_{DD} rising above 4.1V to HO/LO rising
t_{LPHL}	LO turn-off propagation delay	7	7.8	9.3	ns	LI falling to LOL falling
t_{LPLH}	LO turn-on propagation delay	6.6	7.3	8.4	ns	LI rising to LOH rising
t_{HPHL}	HO turn-off propagation delay	9.7	10.6	12.5	ns	HI falling to HOL falling
t_{HPLH}	HO turn-on propagation delay	6.5	7.2	8	ns	HI rising to HOH rising
t_{MON}	Delay matching LO on and HO off	3.5	3.8	4.3	ns	
t_{MOFF}	Delay matching LO off and HO on	1.1	1.15	1.2	ns	
t_{HRC}	HO rise time (0.5 V – 4.5 V)		6		ns	C_L = 1000 pF
t_{LRC}	LO rise time (0.5 V – 4.5 V)		6		ns	C_L = 1000 pF
t_{HFC}	HO fall time (0.5 V – 4.5 V)		2.6		ns	C_L = 1000 pF
t_{LFC}	LO fall time (0.5 V – 4.5 V)		2.6		ns	C_L = 1000 pF
t_{PW}	Minimum input pulse width that changes the output		8		ns	



6 Block diagram



7 Function description

7.1 Input and output

The input pins of the CGD2101WL are independently controlled with TTL input thresholds and can withstand voltages up to 15V regardless of the VDD voltage. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 12V power supply, eliminating the need for a buffer stage.

The output pulldown and pullup resistance of CGD2101WL is optimized for enhancement mode GaN FETs to achieve high frequency and efficient operation. The split outputs of the CGD2101WL offers flexibility to adjust the turn-on and turn-off speed by independently adding additional impedance in either the turn-on path and/or the turnoff path.

If the input signal for either of the two channels, HI or LI, is not used, the control pin must be tied to either VDD or VSS. These inputs must not be left floating.

7.2 Start-up and UVLO

The CGD2101WL has an undervoltage lockout (UVLO) on both the VDD and bootstrap supplies. When the VDD voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient VDD voltage, the UVLO actively pulls the LOL and HOL low. When the VDD voltage is above its UVLO threshold, but the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only HOL is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

7.3 HS negative voltage and bootstrap supply voltage clamping

Due to the intrinsic nature of enhancement mode GaN FETs, the source-to-drain voltage of the bottom switch is usually higher than a diode forward voltage drop when the gate is pulled low. This causes negative voltage on HS pin. Moreover, this negative voltage transient may become even more pronounced due to the effects of board layout and device drain/source parasitic inductances. With high-side driver using the floating bootstrap configuration, negative HS voltage can lead to an excessive bootstrap voltage, which can damage the high-side GaN FET. The CGD2101WL solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5V typical.

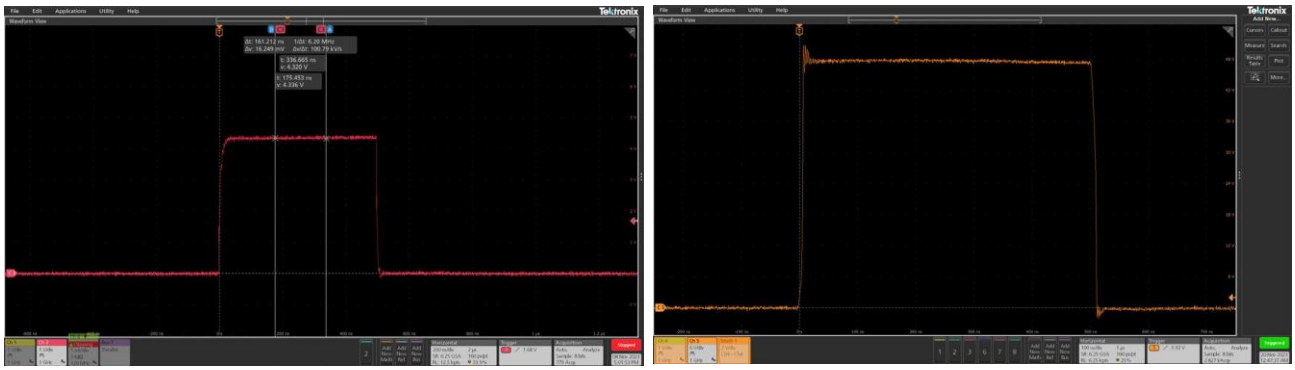
7.4 Level shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver. Typical delay matching between LO and HO is around 3ns.

7.5 Truth table

HI	LI	HOH	HOL	LOH	LOL
L	L	OPEN	L	OPEN	L
L	H	OPEN	L	H	OPEN
H	L	H	OPEN	OPEN	L
H	H	H	OPEN	H	OPEN

7.6 Typical testing waveforms



(Left) High Side GaN Gate Waveform with EPC2088 GaN Load @ 500KHz; (Right) HS: Switch Node Waveform with EPC2088 GaN Load @ 48V to 12V DCDC Buck System, 500KHz

8 Layout guidelines

Small gate capacitance and Miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt, coupled with a low gate threshold voltage and limited

headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some recommendations:

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This decreases the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs must be placed close to the driver.

2. The second high current path includes the bootstrap capacitor, the local ground referenced VDD bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

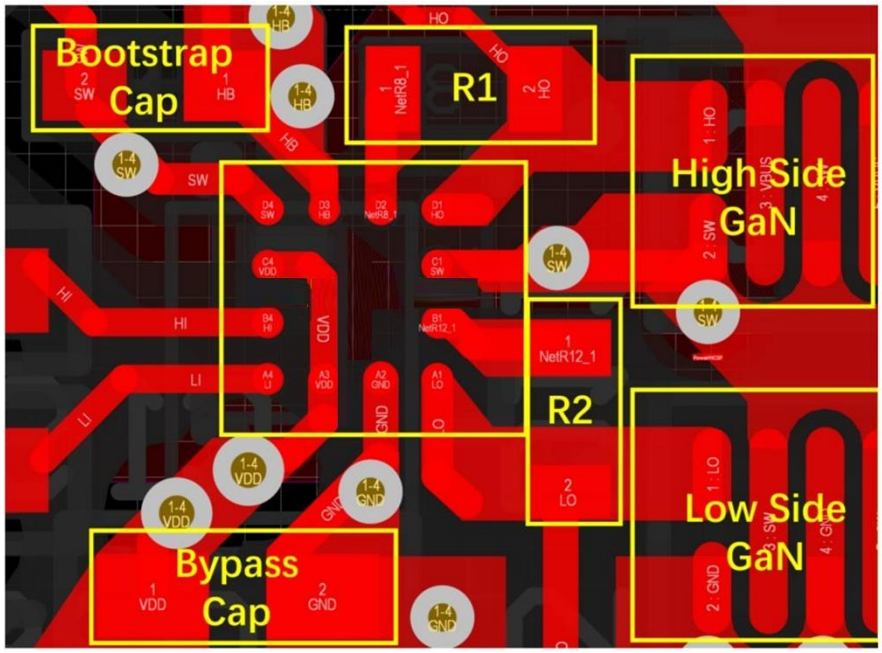
3. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. We recommend connecting the HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.

4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form an LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

5. Low ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak current being drawn from VDD during turn-on of the FETs. The inductance of vias can impose excessive ringing on the IC pins.

6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low ESR ceramic capacitors adjacent to the GaN FETs.

A four-layer or higher layer count board is required to reduce the parasitic inductance of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

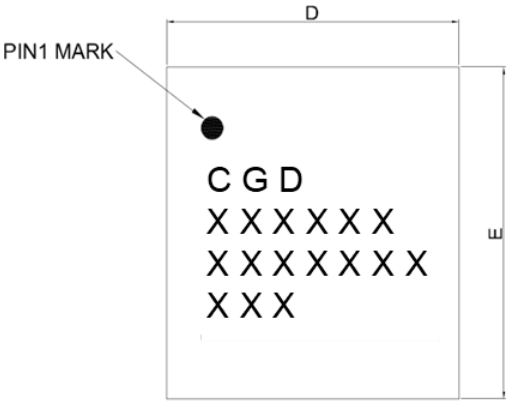


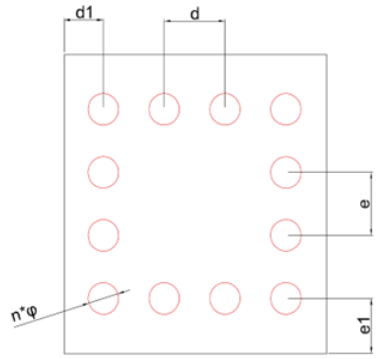
9 Package information

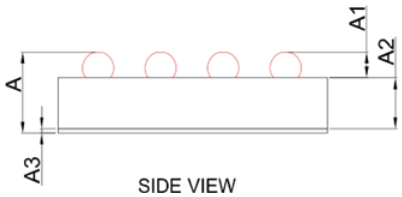
Orderable Device	Package Type	Op Temp (°C)	Eco Plan	Package Marking	Packing Option
CGD2101WL	WLCSP	-40 to 125	RoHS & PAHs	CGD XXXXXX XXXXXXX XXX	Tape and Reel, 3000pcs/reel

RoHS: PowerX defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances.

PAHs: PowerX defines "PAHs" to mean semiconductor products that are compliant with the current EU PAHs requirements for 18 PAHs substances.







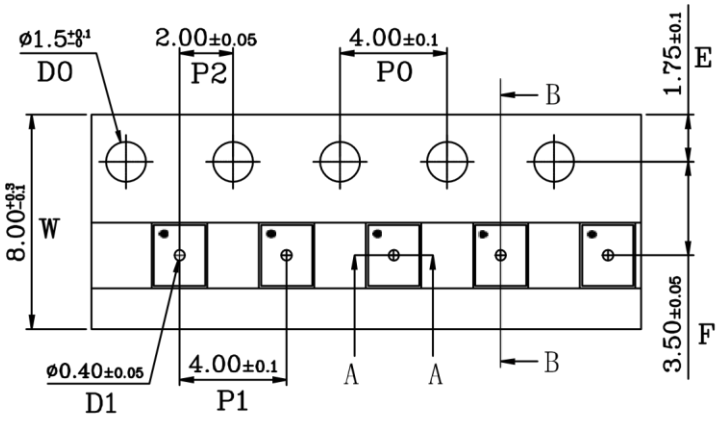
SIDE VIEW

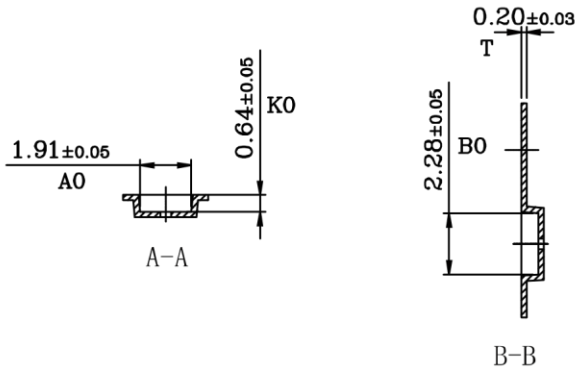
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

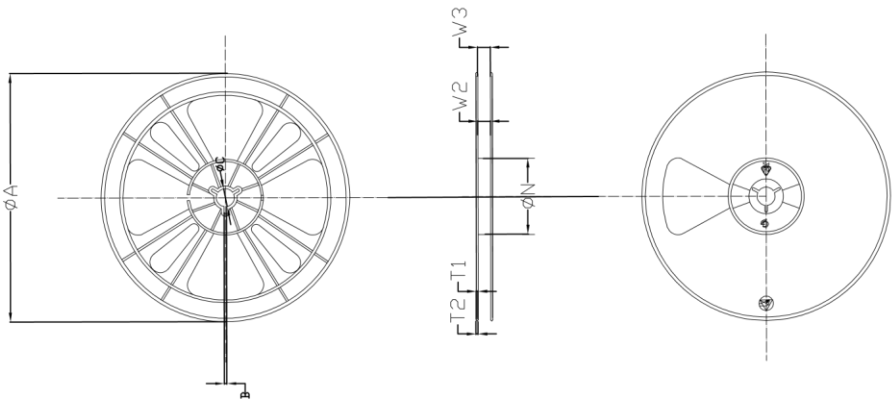
SYMBOL	ITEM	MIN	NOM	MAX
A	PACKAGE HEIGHT	0.460	0.501	0.542
A1	BALL HEIGHT	0.137	0.161	0.185
A2	WAFER THICKNESS	0.302	0.315	0.329
A3	BACKSIDE FILM THICKNESS	0.022	0.025	0.028
Φ	BALL DIAMETER	0.180	0.200	0.220
D	PACKAGE SIZE X	1.705	1.725	1.745
E	PACKAGE SIZE Y	1.875	1.895	1.915
d	MIN BALL PITCH X		0.400	
d1	MIN BALL CENTER TO PACKAGE SIZE X AXIS		0.257	
e	MIN BALL PITCH Y		0.400	
e1	MIN BALL CENTER TO PACKAGE SIZE Y AXIS		0.347	
n	BALL COUNT		12	

10 Tape and reel information

Type/Size					(UNIT:mm)				
Type	W	P1	E	F	D0	D1	P0	P2	10P0
Size	$8.00^{+0.3}_{-0.1}$	4.00±0.10	1.75±0.10	3.5±0.05	$1.50^{+0.10}_{-0}$	0.4±0.05	4.0±0.1	2±0.05	40±0.2
Type	A0	A1	B0	B1	K0	K1	T		
Size	1.91±0.05		2.28±0.05		0.64±0.05		0.20±0.03		







Item	Value&Tolerance
A	179±1.0
B	2.0±0.2
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2+1.0
T1	1.2±0.2
T2	1.5±0.2

11 Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.8	2025-6-5	0.8 version release