High-Performance 100-V GaN Transistor with Integrated Gate Driver

General description

The CGR1101 is a high-performance and highly reliable 100-V enhancement-mode GaN transistor with integrated gate driver, optimized for high switching frequency applications, including LiDAR, Time-of-Flight (ToF), and power converter. The minimum 1-ns input pulse width makes higher power/current allowable in these applications to improve mapping range and resolution. The extremely small propagation delay of 3.3ns significantly improves the control loop response time and thus overall performance of the power converters. Split output allows the drive strength and switching time to be adjusted through external resistors between OUT+ and OUT-.

The power GaN transistors in CGR1101, have 100-V drain-source blocking voltage and typical $R_{DS(ON)}$ of 7 mΩ.

CGR1101 features undervoltage lockout (UVLO) and over-temperature protection (OTP) to ensure the GaN transistor is not damaged in overload or fault conditions.

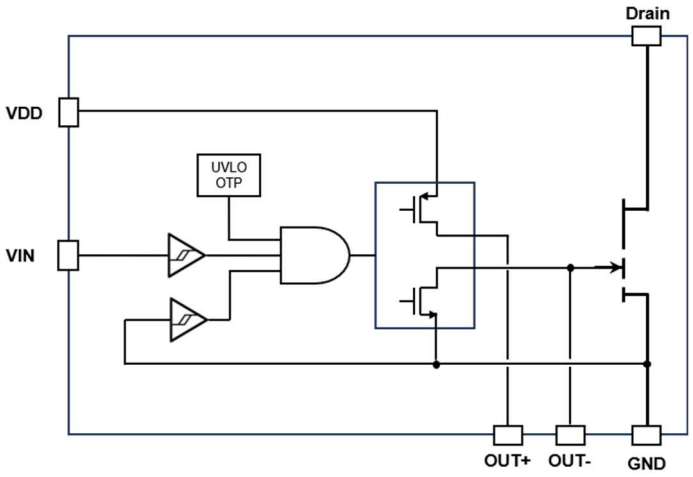
CGR1101 is available in a compact 5 x 6 mm DFN package for a minimized parasitic inductance.

Features

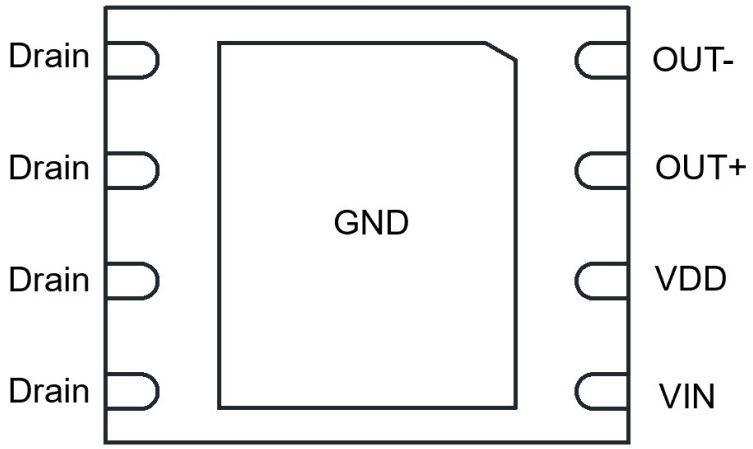
- GaN transistors with integrated gate drive
- 100 V continuous voltage rating
- Zero reverse recovery charge
- Typ./Max. $R_{DS(ON)}$ = 5.5/7mΩ
- 7-A pull-up and 5-A pull-down current
- Programmable turn-on dV/dt
- 5 x 6 mm footprint with large cooling pad
- UVLO and over-temperature protection
- Recommended single 5-V supply voltage

Typical applications

- Automotive LiDAR
- Vehicle Occupant Detection Sensor
- Class-E Wireless Charger
- GaN-Based Synchronous Rectifier
- DC/DC converter
- BLDC driver



Pin configuration and functions



Package Top View

Name	I/O	Description
Drain	P	Drain of GaN transistor.
VDD	P	Gate driver supply voltage. Locally bypass this pin to GND with a ceramic capacitor
VIN	I	PWM signal logic input
OUT+	O	Gate driver turn-on slew-rate set pin (using R_{gon})
OUT-	O	Gate driver turn-on slew-rate set pin (using R_{gon})
GND	G	Gate driver ground. Internally connected to Source of GaN transistor

I = Input, O = Output, P = Power, G = Ground, NC = No Connect

Ordering information

Ordering Code	Package	Marking	Packing
CGR1101	DFN5*6	CGR1101	Reel

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1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute maximum ratings* may cause permanent damage to the device.

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate driver supply voltage	V_{DD}	0	-	5.75	V	
Input pin voltage	V_{IN}	-0.3	-	6	V	
OUT+, OUT- pin voltage	V_{OUT}	-0.3	-	6	V	
Drain-source voltage	$V_{DS, max}$	-	-	100	V	V_{GS} = 0 V, I_D = 600 μA
Continuous current, drain-source	I_D	-	-	29	A	T_c = 25 °C
Pulsed current, drain-source [1]	$I_{D, pulse}$	-	-	125	A	T_c = 25 °C
Operating temperature	T_j	-40	-	150	°C	
Storage temperature	T_{stg}	-55	-	150	°C	

Notes

1. Pulse width = 100 μs.

2 Recommended operating conditions

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate driver supply voltage	V_{DD}	4.75	5	5.25	V	
Input pin voltage	V_{IN}	0	-	V_{DD}	V	
OUT+, OUT- pin voltage	V_{OUT}	-5	-	V_{DD}		
Junction temperature	T_j	-40	-	+125	°C	

3 Thermal characteristics

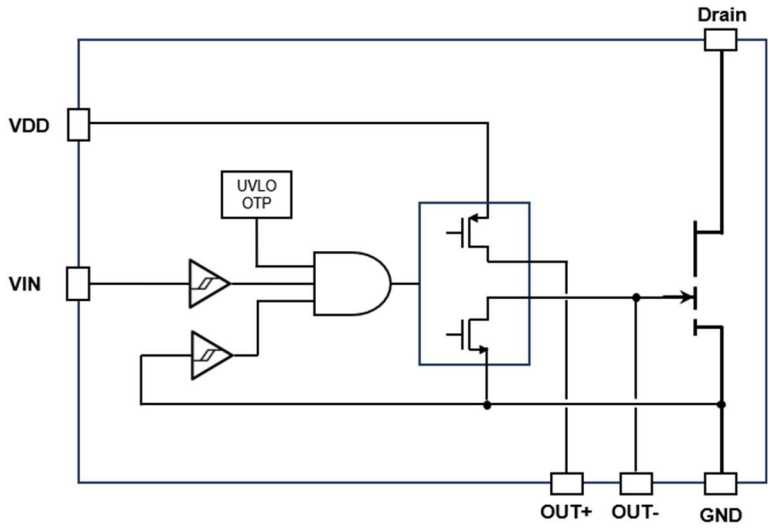
Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	–	1.6	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

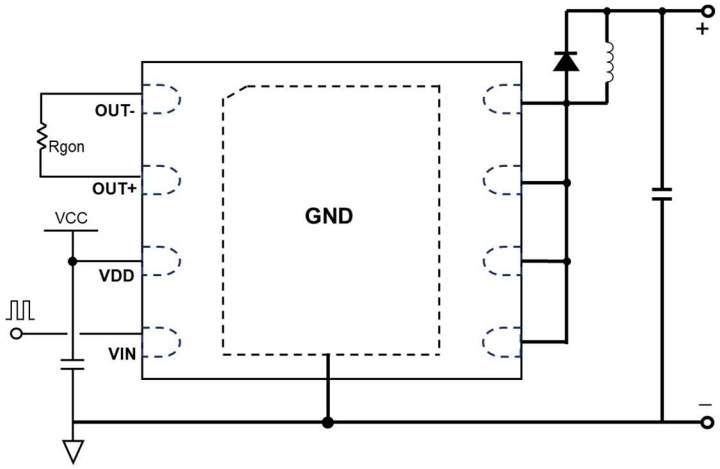
Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only.
Unless otherwise specified, V_{DD} = 5 V

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
DC Characteristics						
V_{DD} quiescent current	$I_{VDD,q}$	64	88	128	μA	V_{IN} = 0 V
V_{DD} operating current	$I_{VDD,op}$	-	5	-	mA	f_{SW} = 1 MHz; V_{DS} = open
Under-voltage Lockout	$V_{DD,UVLO}$	3.9	4.1	4.2	V	
V_{DD} UVLO hysteresis	V_{DD-HYS}	-	200	-	mV	
Over temperature shutdown threshold	T_{OTP}	-	164	-	°C	
Over temperature hysteresis	$V_{OTP-HYS}$	-	20	-	°C	
Input DC Characteristics						
Input logic high threshold (rising edge)	V_{IH}	1.6	-	2.5	V	
Input logic low threshold (falling edge)	V_{IL}	1.1	-	1.9	V	
Input logic hysteresis	V_{IHYS}	0.4	-	0.9	V	
Input pin pull-down resistance	R_{IN}	100	180	200	kΩ	To GND
Output DC Characteristics						
Peak source current	I_{OH}	-	7	-	A	
Peak sink current	I_{OL}	-	5	-	A	
Switching Characteristics						
Startup Time, VDD rising above UVLO	T_{start}	40	50	70	us	V_{IN}= V_{DD}, V_{DD} rising above 4.4V to OUT+ rising
Turn-on propagation delay	T_{ON}	2	3.3	4	ns	V_{IN} to OUT+, 220pF load
Turn-off propagation delay	T_{OFF}	2	3.3	4	ns	V_{IN} to OUT-, 220pF load
Rise time	T_R	-	650	-	ps	0Ω series 220pF load
Fall time	T_F	-	650	-	ps	0Ω series 220pF load
Minimum input pulse width	T_{min}	-	1.25	-	ns	0Ω series 220pF load
GaN FET Characteristics						
Drain-source leakage current	I_{DSS}	-	1.5	14	μA	V_{DS} = 80V; V_{IN} = 0; T_j = 25°C
Drain-source on-state resistance	$R_{DS(on)}$	-	5.5	7	mΩ	V_{IN} = 5V; I_D = 16A; T_j = 25 °C
		-	10	-	mΩ	V_{IN} = 5V; I_D = 16A; T_j = 125 °C
Source-drain reverse voltage	V_{SD}	-	1.4	-	V	V_{IN} = 0 V; I_{SD} = 0.5 A
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 0.5 A; V_{DS} = 50 V
Output capacitance	C_{oss}	-	220	-	pF	V_{IN} = 0V; V_{DS} = 50V; f = 1 MHz
Effective output capacitance, energy related	$C_{o(er)}$	-	340	-	pF	V_{IN} = 0 V; V_{DS} = 0 to 50 V
Effective output capacitance, time related	$C_{o(tr)}$	-	500	-	pF	
Output charge	Q_{OSS}	-	25	-	nC	

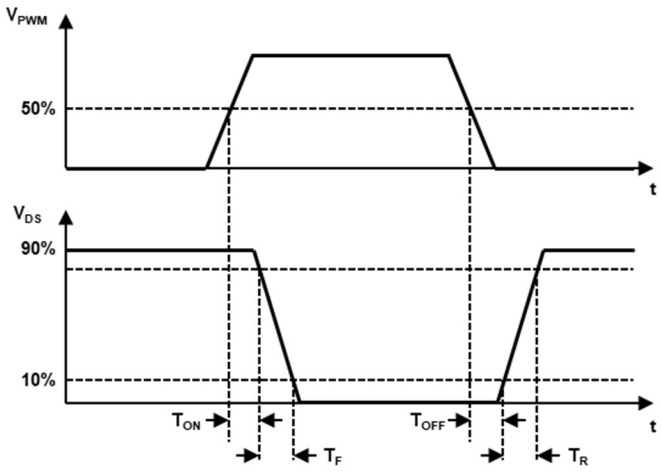
5 Block diagram



6 Switching waveforms



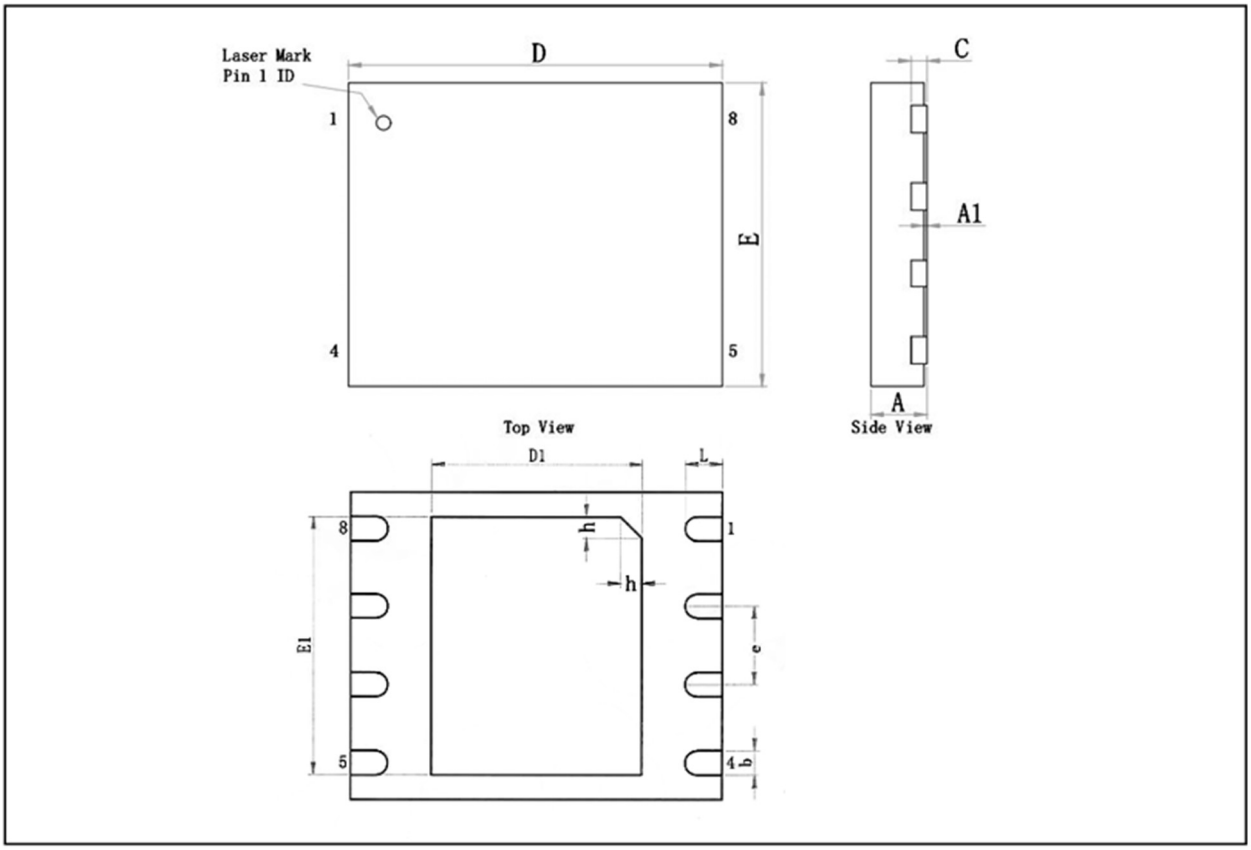
Inductive-load switching circuit



Propagation delay and rise/fall time definitions

7 Package outlines

Dimensions(mm)			
Symbol	Min.	Nom.	Max.
A	0.8	0.85	0.9
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c		0.203REF	
D	5.90	6.00	6.10
D1	3.30	3.40	3.50
E	4.90	5.00	5.10
E1	4.10	4.20	4.30
h	0.30	0.35	0.40
L	0.55	0.60	0.65
e		1.270BSC	



8 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-12-3	1.0 version release